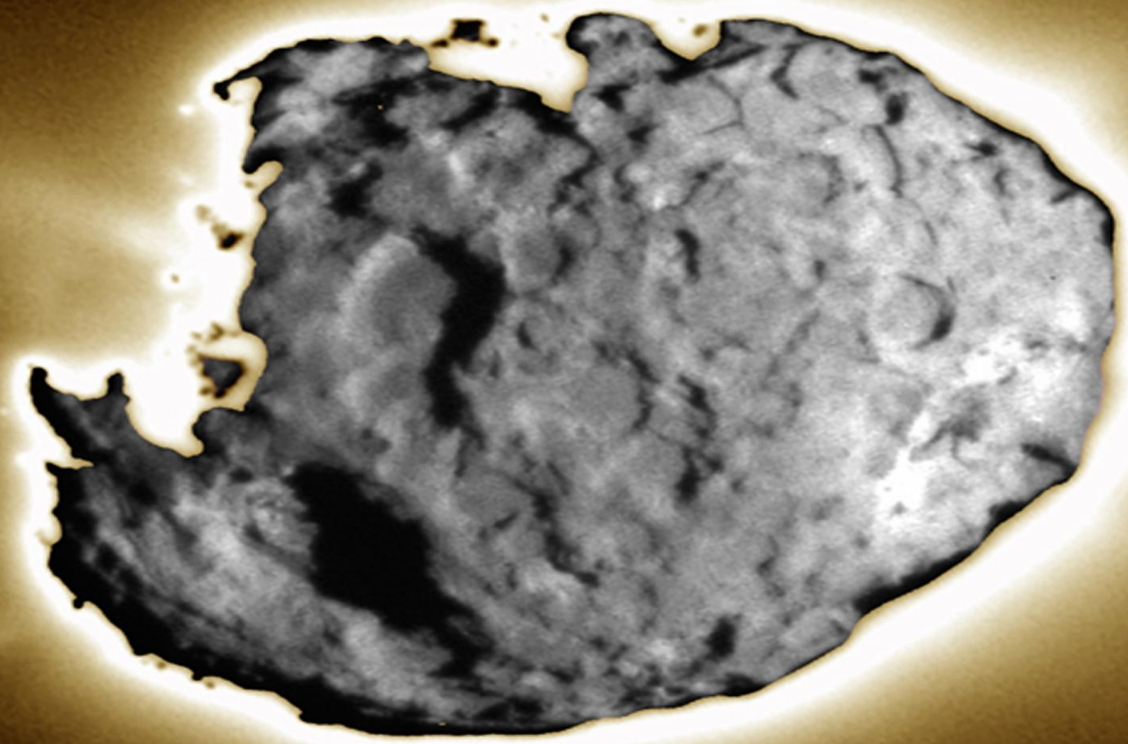
ION IMPLANTATION



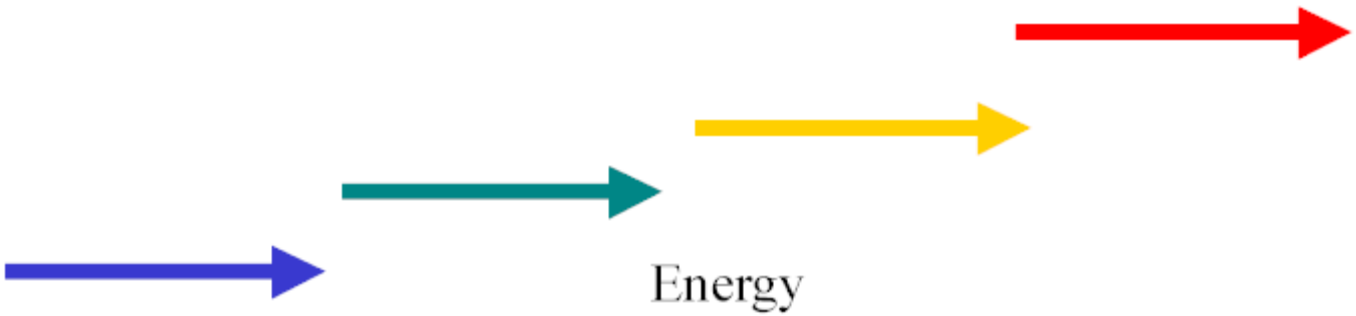
BY

AJAL.A.J

Introduction: What is a Plasma

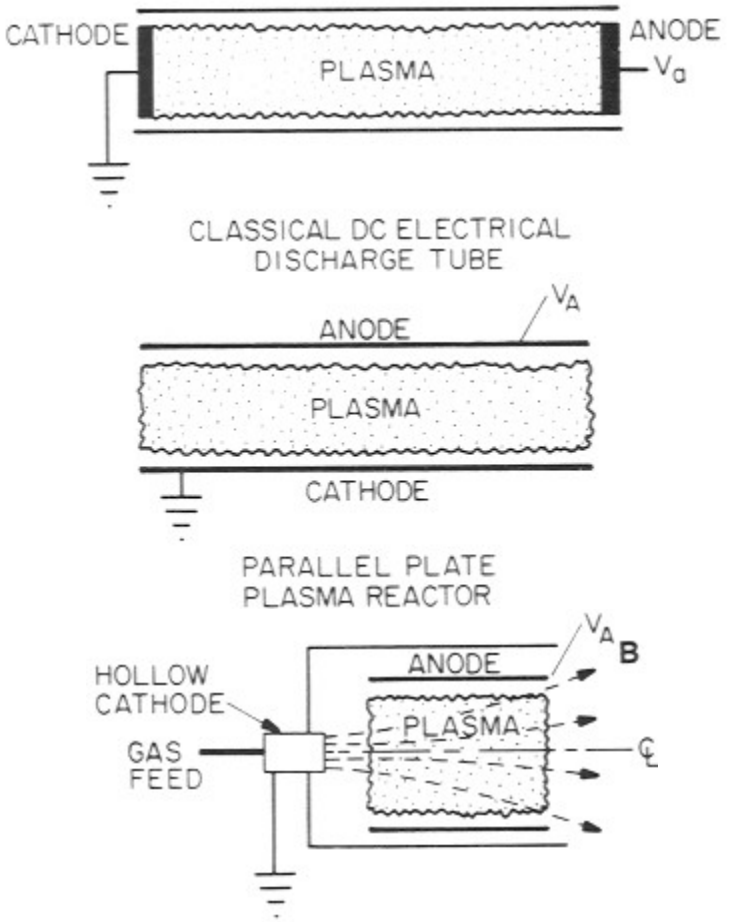
- States of Matter (Ancient View)
  - Earth, Water, Wind, Fire

- States of Matter (Modern View)
  - Solid, Liquid, Gas, Plasma



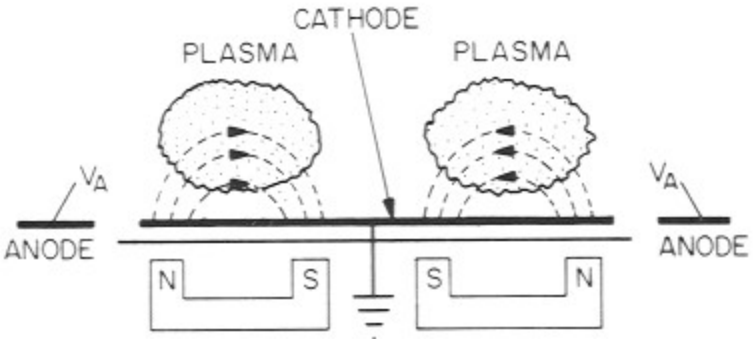
Various types of Plasma Sources

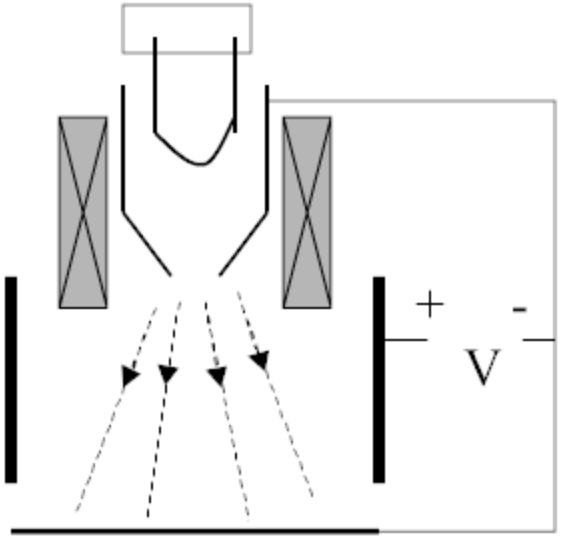
- DC Discharges
  - Without Magnetic Confinement
    - Discharge Tubes
    - Parallel Plate
    - Hollow Cathode



Various types of Plasma Sources

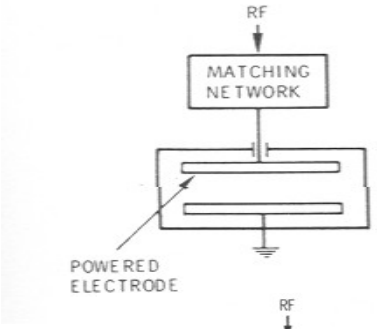
- With Magnetic Confinement
  - Magnetron (variety)
  - PIG Discharges

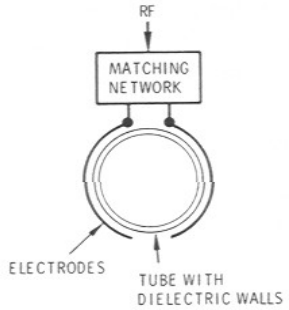


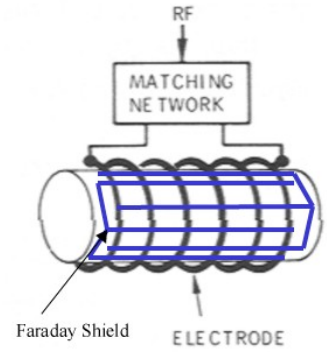


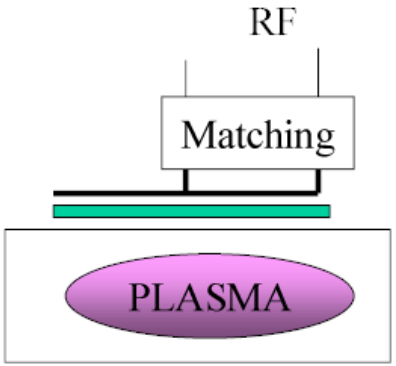
Various types of Plasma Sources

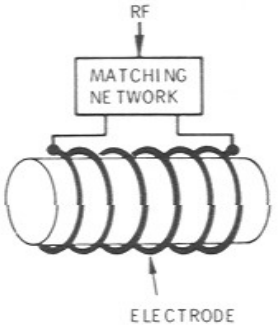
- ✓ RF Discharges
  - Capacitively Coupled
  - Inductively Coupled



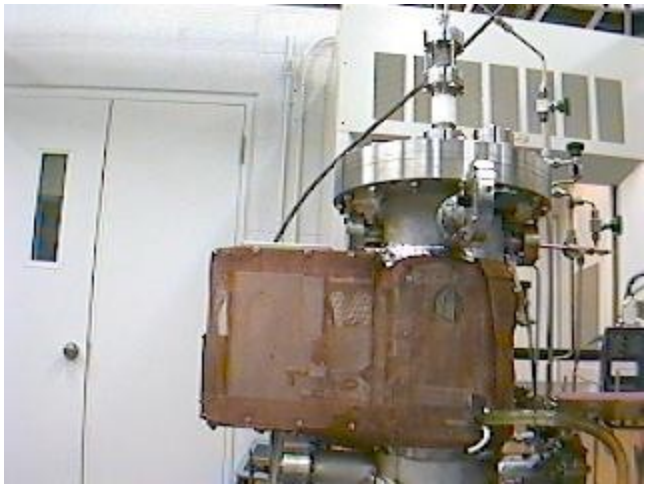


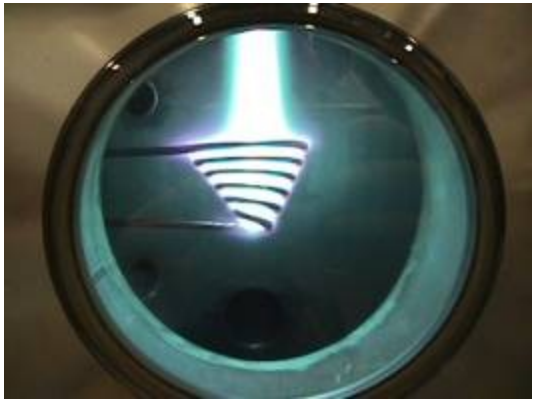


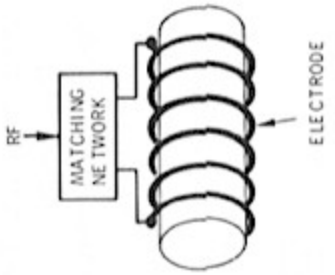


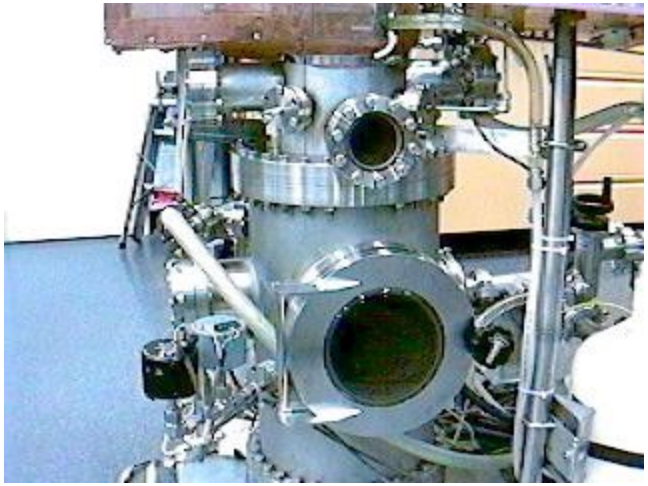


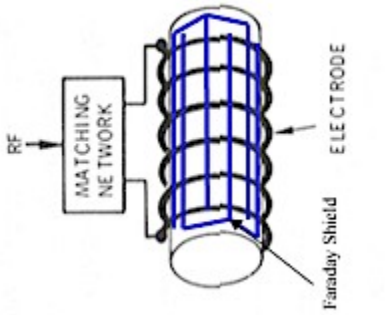
Various types of Plasma Sources





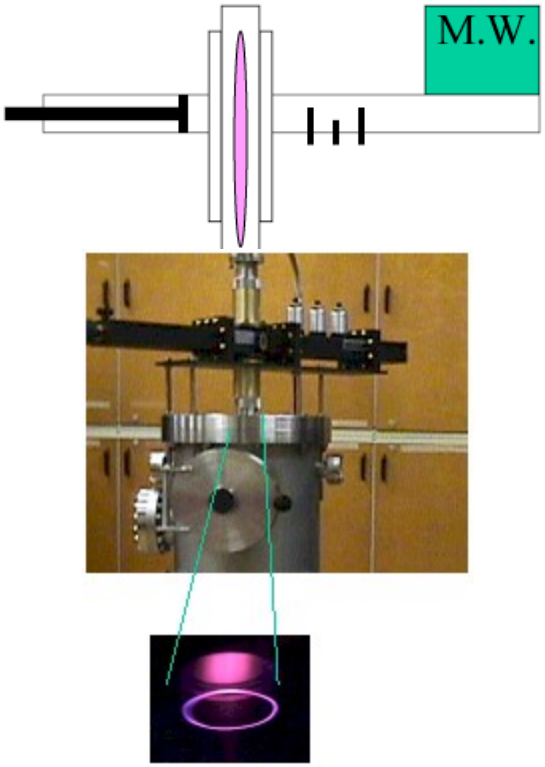


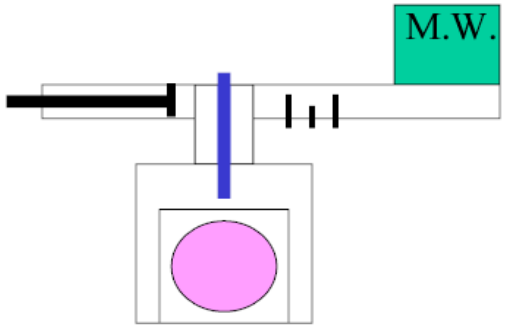




Various types of Plasma Sources

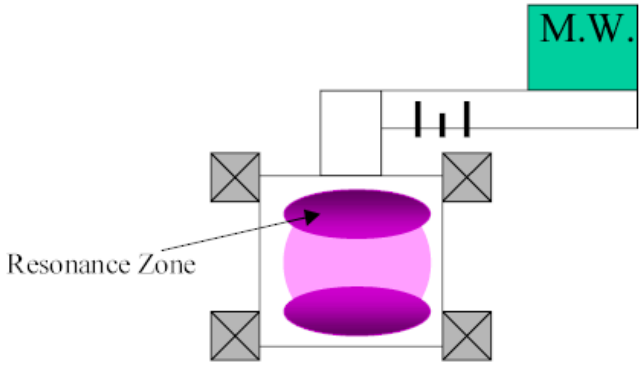
- ✓ Microwave Discharge
  - Remote Plasma
  - Microwave Cavity





Various types of Plasma Sources

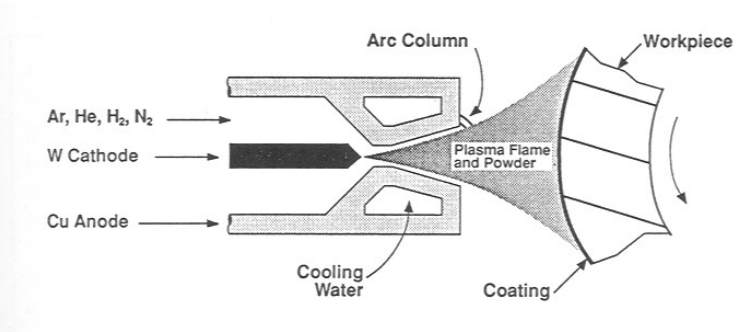
- Microwave Discharge
  - Electron Cyclotron Resonance (ECR)

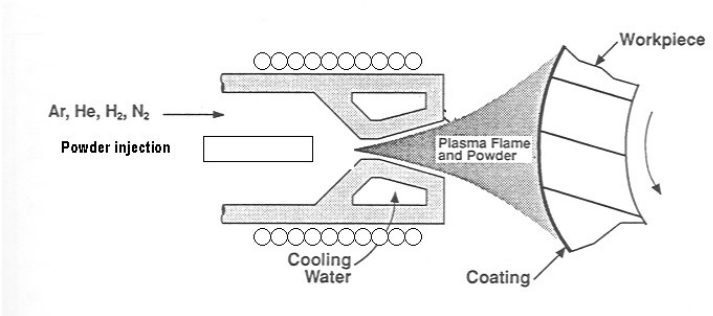


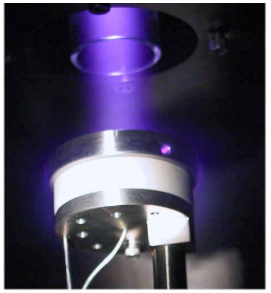
- The condition when electron cyclotron frequency, $\omega_e = eB/m_e$, is the same as the frequency of the electric field oscillations is called ECR. The result is that electrons gain energy from the field constantly.
  - The resonance condition for electrons at 2.45 GHz corresponds to B = 875 Gauss

Various types of Plasma Sources

- Plasma Torches
  - DC
  - RF
  - Microwave





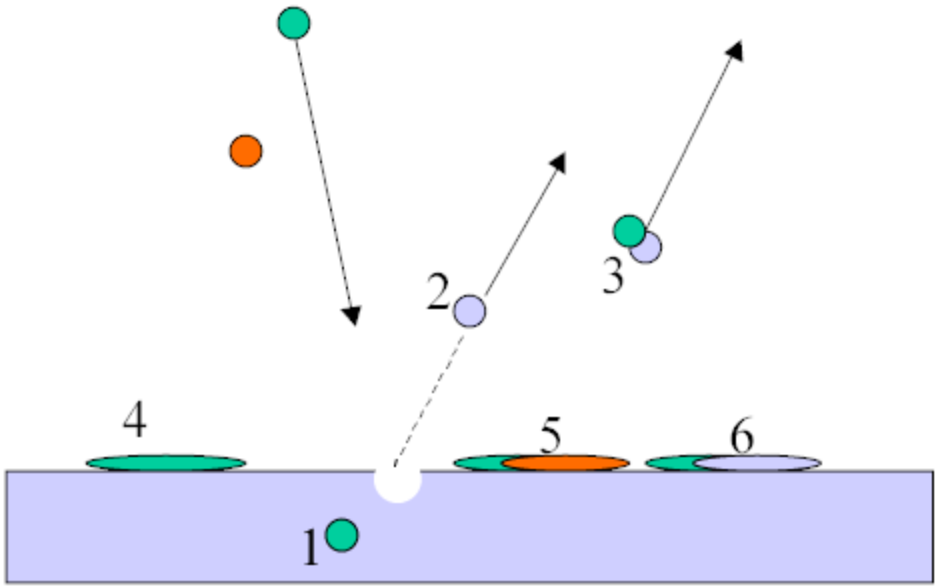


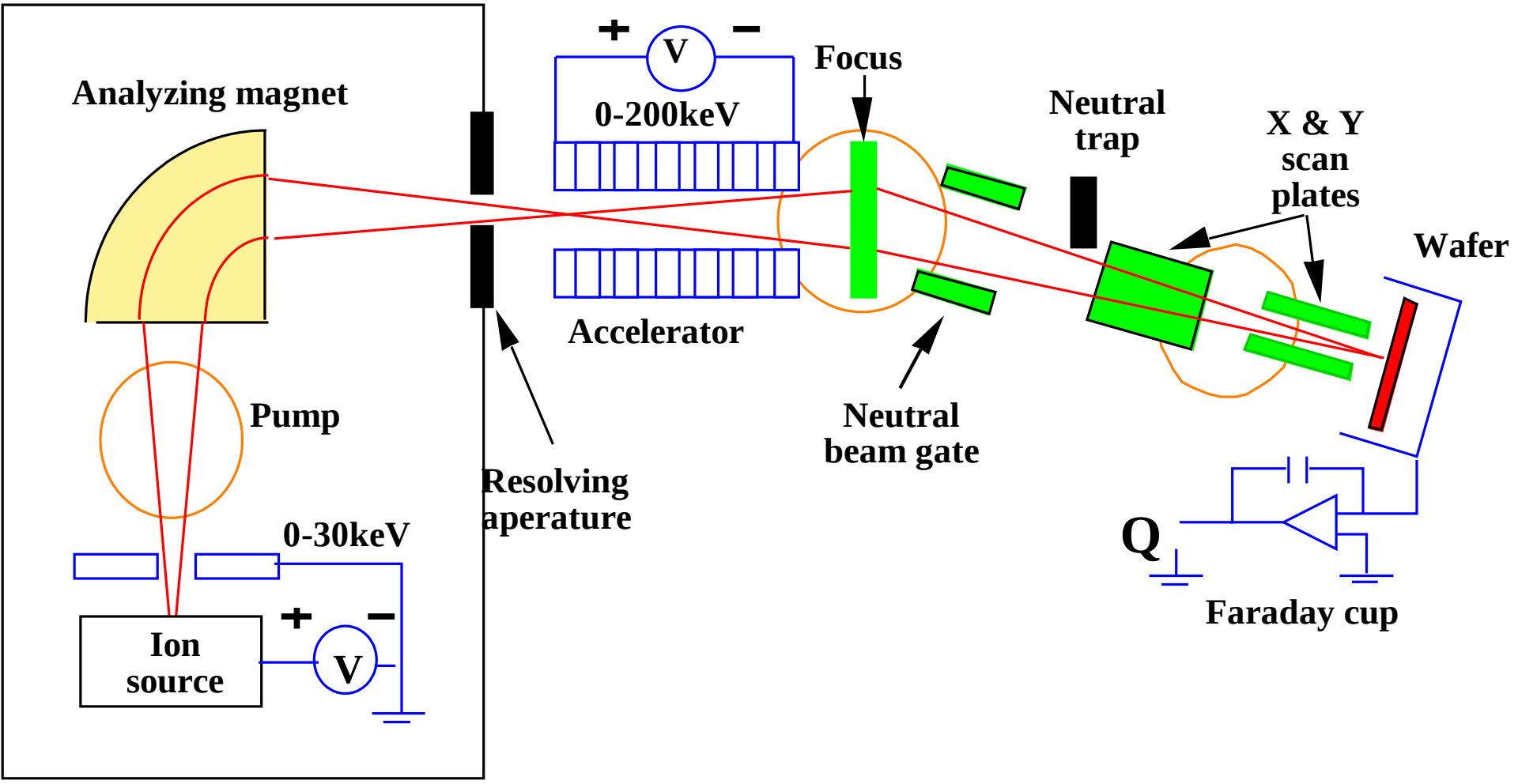
Disadvantages of Plasma Surface Engineering

- Slow
- Expensive

Plasma-Based Processes

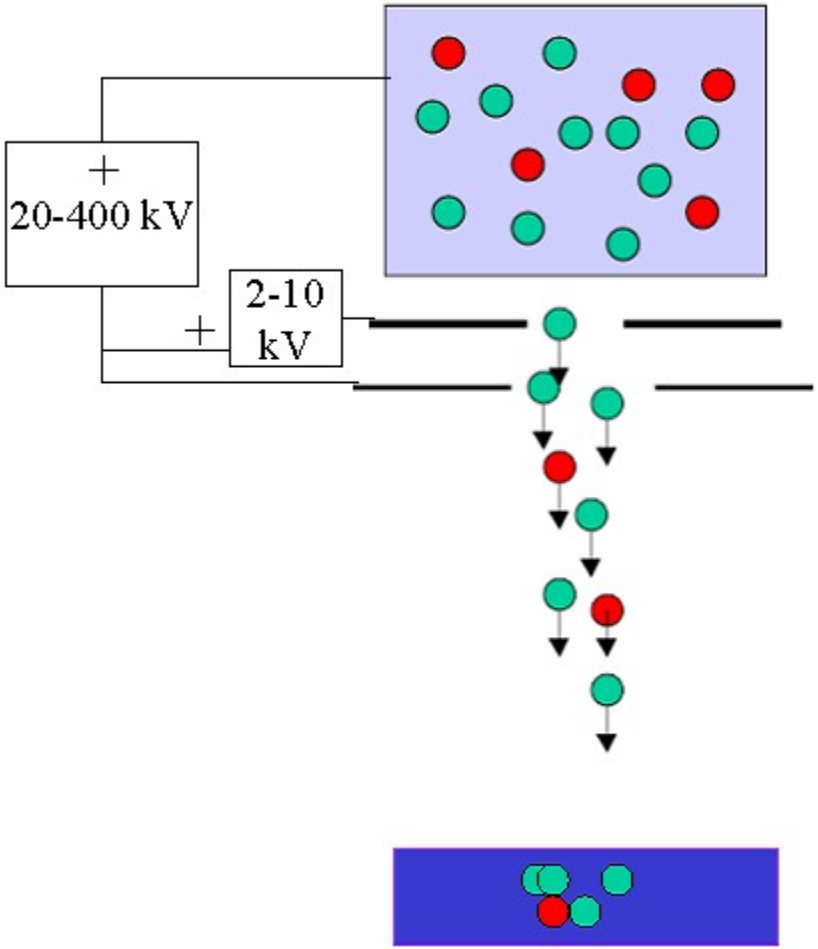
- Implantation (1)
- Sputtering(2)
- Etching (3)
- Deposition
  - Physical (4)
  - Chemical (5,6)
- Others
  - Arc evaporation
  - e-beam




Analyzing magnet
+
V
−
0-200keV
Focus
Neutral
trap
X & Y
scan
plates
Wafer
Accelerator
Pump
Resolving
aperature
Neutral
beam gate
0-30keV
Q
Ion
source
+
V
−
Faraday cup

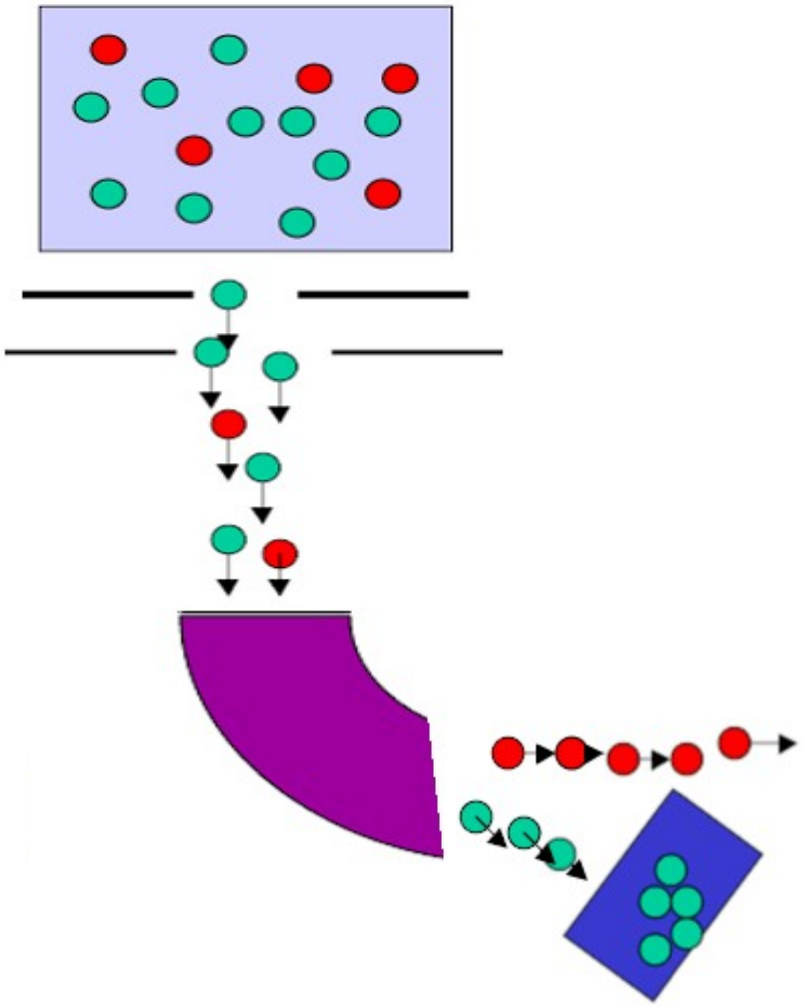
Ion Implantation (conventional)

- Plasma Created
- Ions extracted from plasma
- Ions accelerated to high energy
- Ions Implanted
  - non selective



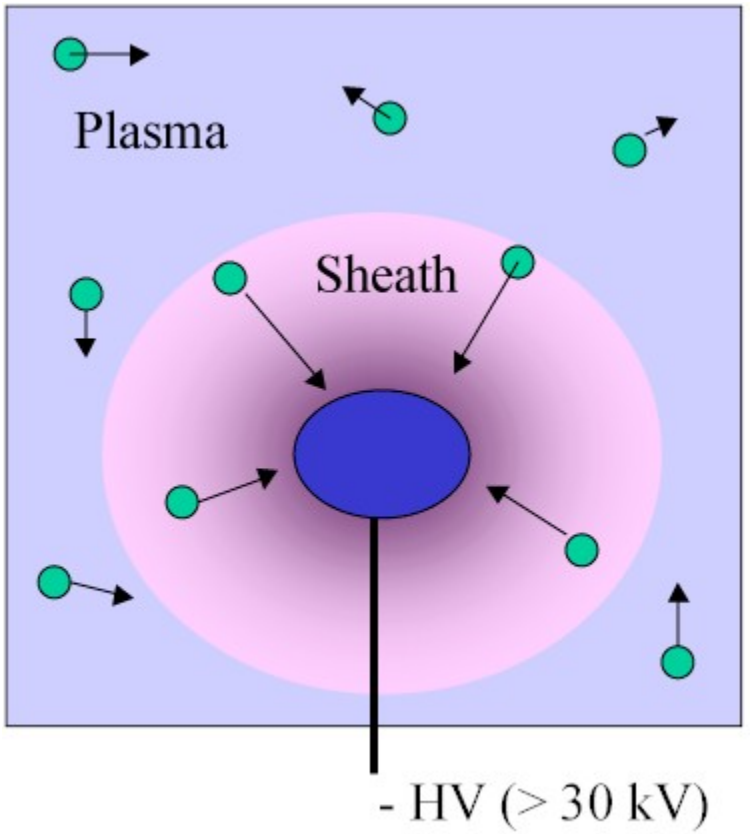
Ion Implantation (conventional)

- Plasma Created
- Ions extracted from plasma
- Ions accelerated to high energy
- Ions Mass Separated Magnetically
- Selected Ions Implanted



Ion Implantation (Plasma-Based)

- Plasma Created
- Object Immersed in Plasma
- Object Biased to Negative Voltage
  - Electrons repelled
  - Ions accelerated and interact with object

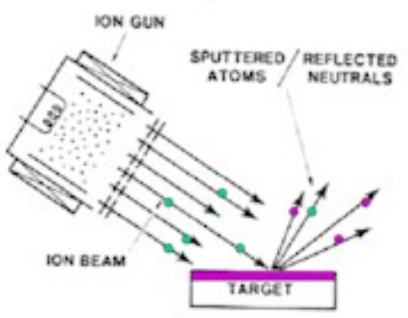


Applications of Ion Implantation

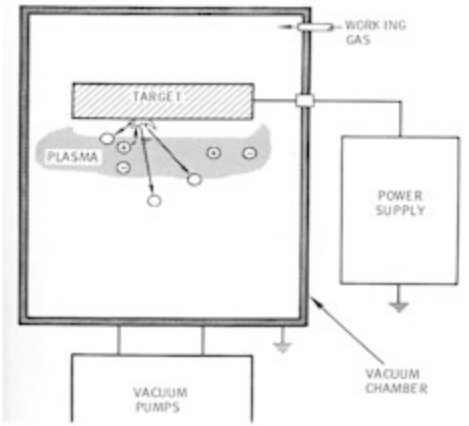
- Metal parts on heart valves are ion implanted by carbon to make them biocompatible
- Radioisotops are implanted in prosthesis for localized radiotherapy

Sputtering

- Ion Beam Assisted



- Plasma-Based Sputtering (immersion)

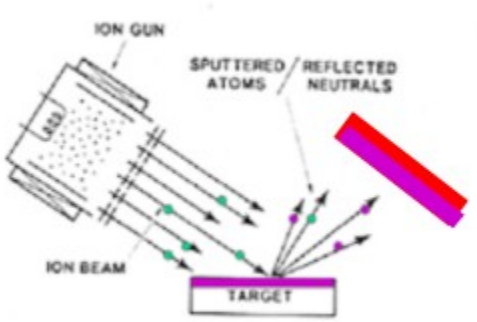


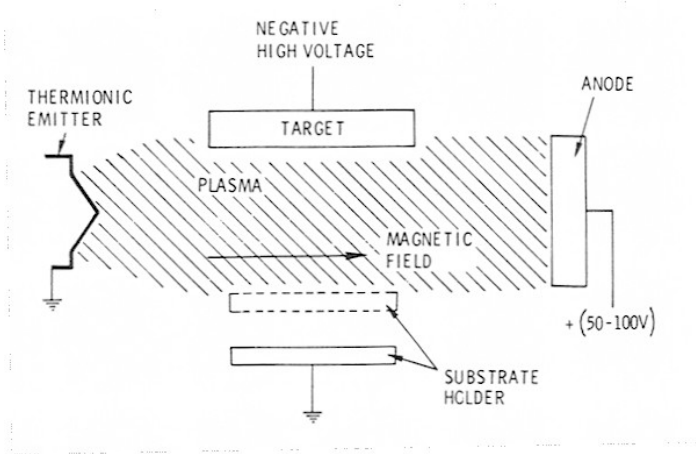
Plasma-Based Deposition

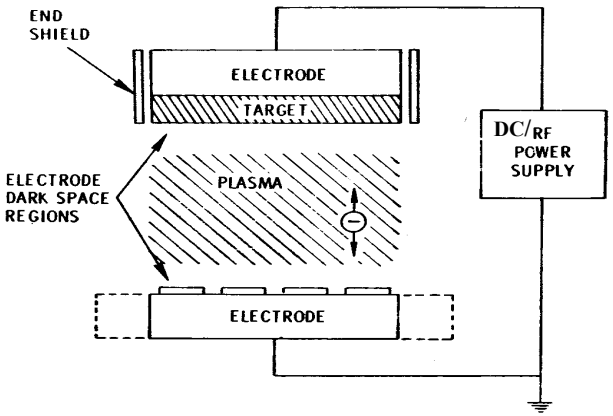
- Physical Vapor Deposition
  - Sputter Deposition
  - e-beam deposition
- Plasma Enhanced Chemical Vapor Deposition
- Deposition by Plasma Spray
- Deposition by Laser Ablation

Sputter Deposition

- Ion Plating
- Ion Beam Assisted Deposition
- Planar Diode
  - DC
  - RF
- Triode Discharge

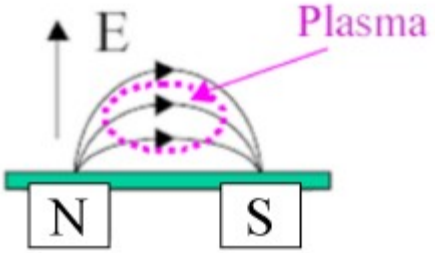


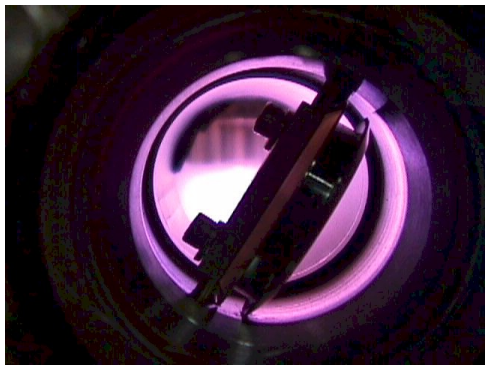


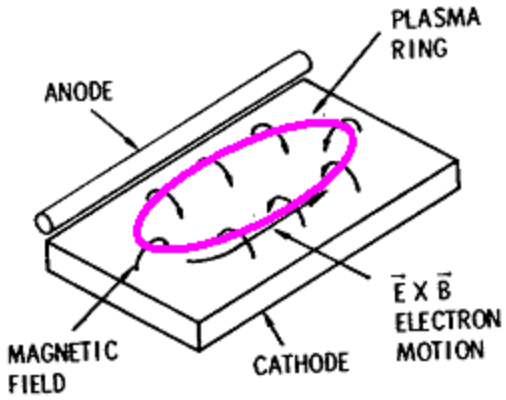


Sputter-Deposition

- Magnetrons
  - DC
  - RF

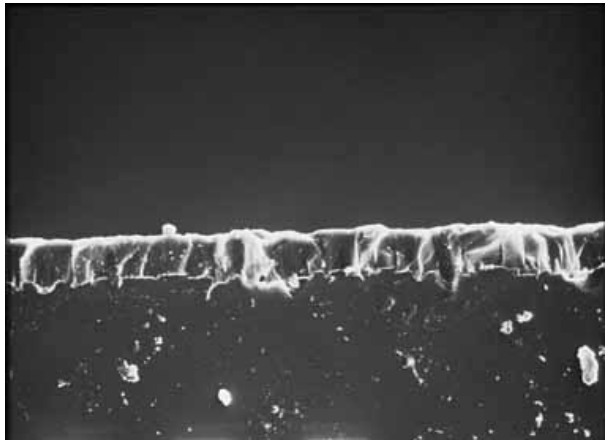


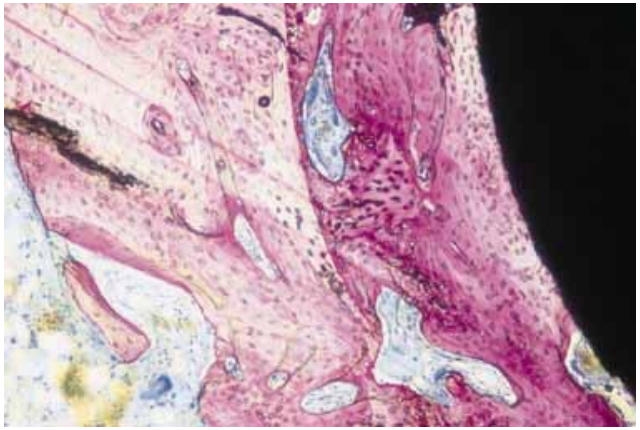




Applications of Sputter Deposition

- Sputter deposition can be used for coating medical implants. It allows insulating films, such as calcium phosphate, to be deposited uniformly over large areas. The coating is relatively dense, adheres well to the substrate, and closely resembles that of the object. Sputtering can also coat materials that are sensitive to heat.
- Example of rf magnetron sputtering deposited thin (1μm) films of hydroxyapatite onto titanium.





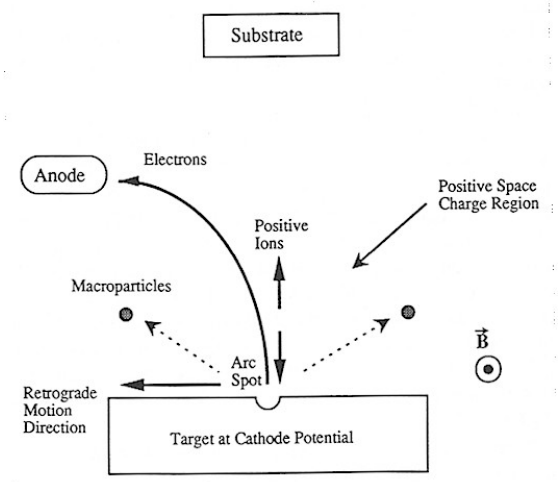
A cross-sectional view of an in vivo calcium-phosphate-coated implant nine weeks after it was put in place. The pink areas show natural bone, while the black area is the implant (magnification x40).

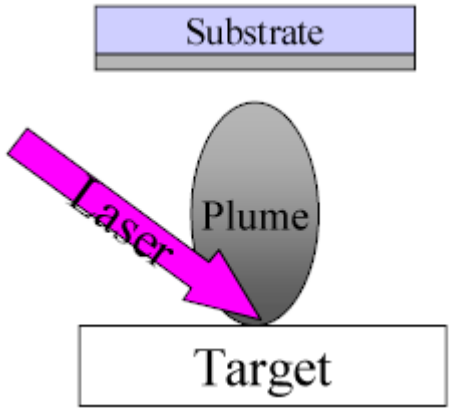
PECVD

- Plasma Produces Significant Radicals
  - Allows deposition at lower temperatures
  - Allows deposition of new materials
- All Types of Plasma sources can be used for applications to PECVD
  - Lower frequency sources => higher ion energy
  - Higher frequency sources=> stable discharge

Other Deposition Techniques

- Cathodic Arc Discharge
  - Arc is a self sustained current channel
- Laser Ablation
- Plasma Spray





Semiconductor basics

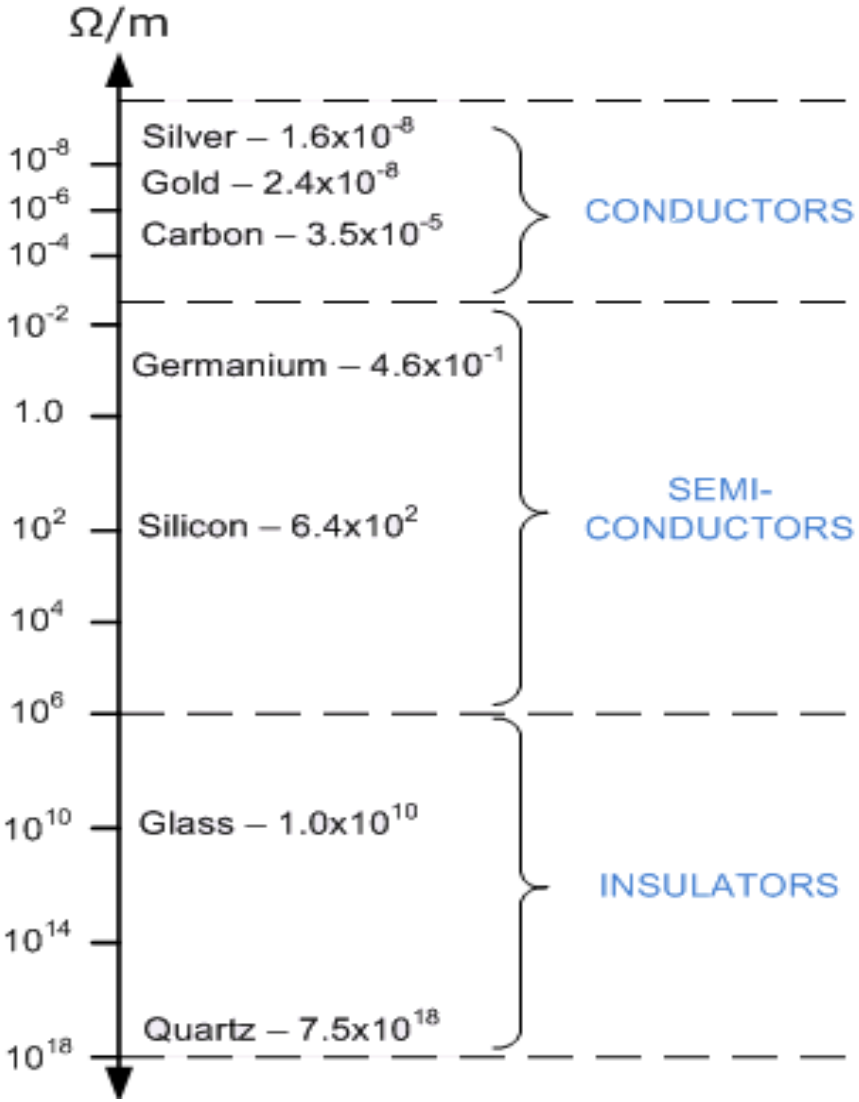


FIGURE 1 : Resistivity chart

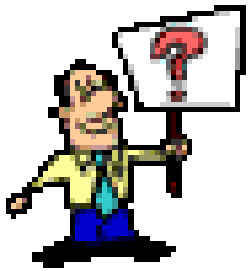
- resistance

$$R = \frac{V}{I}$$

- resistivity ,f(T)

$$\rho = R\frac{A}{\ell}$$

- conductor
- insulator
- semiconductor

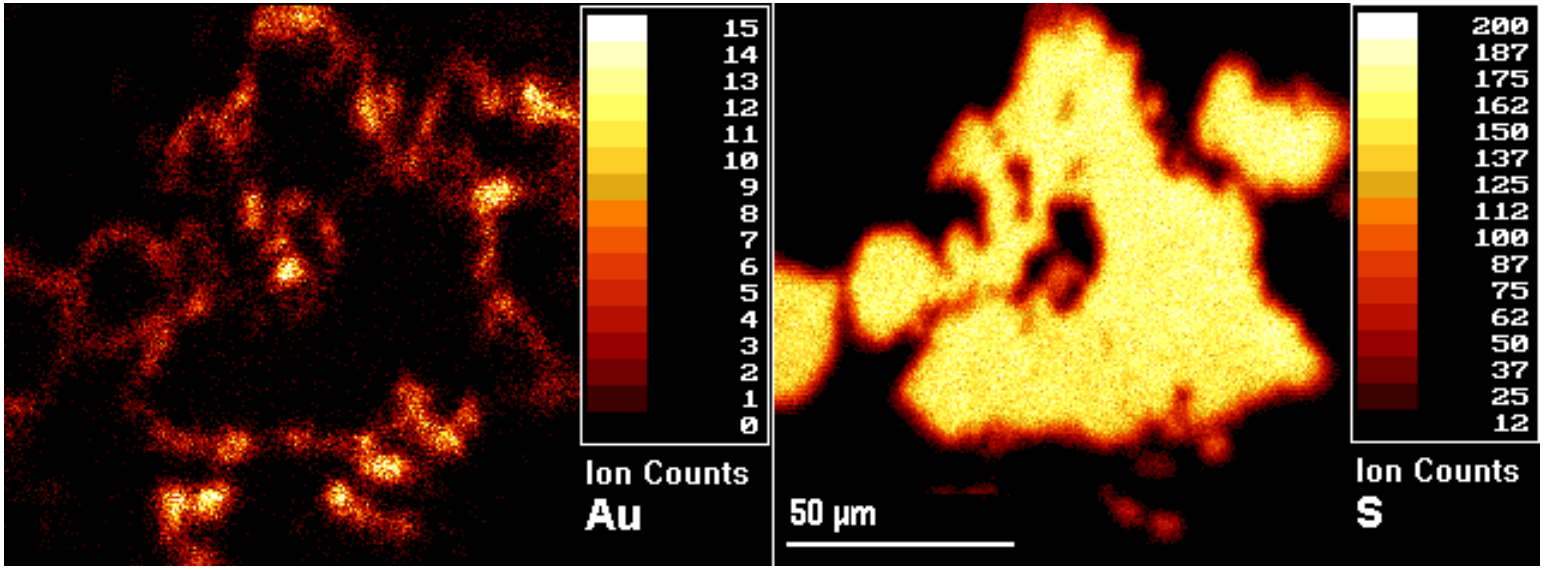


Prediction is very difficult,
Especially if it's about
the future

Niels Bohr

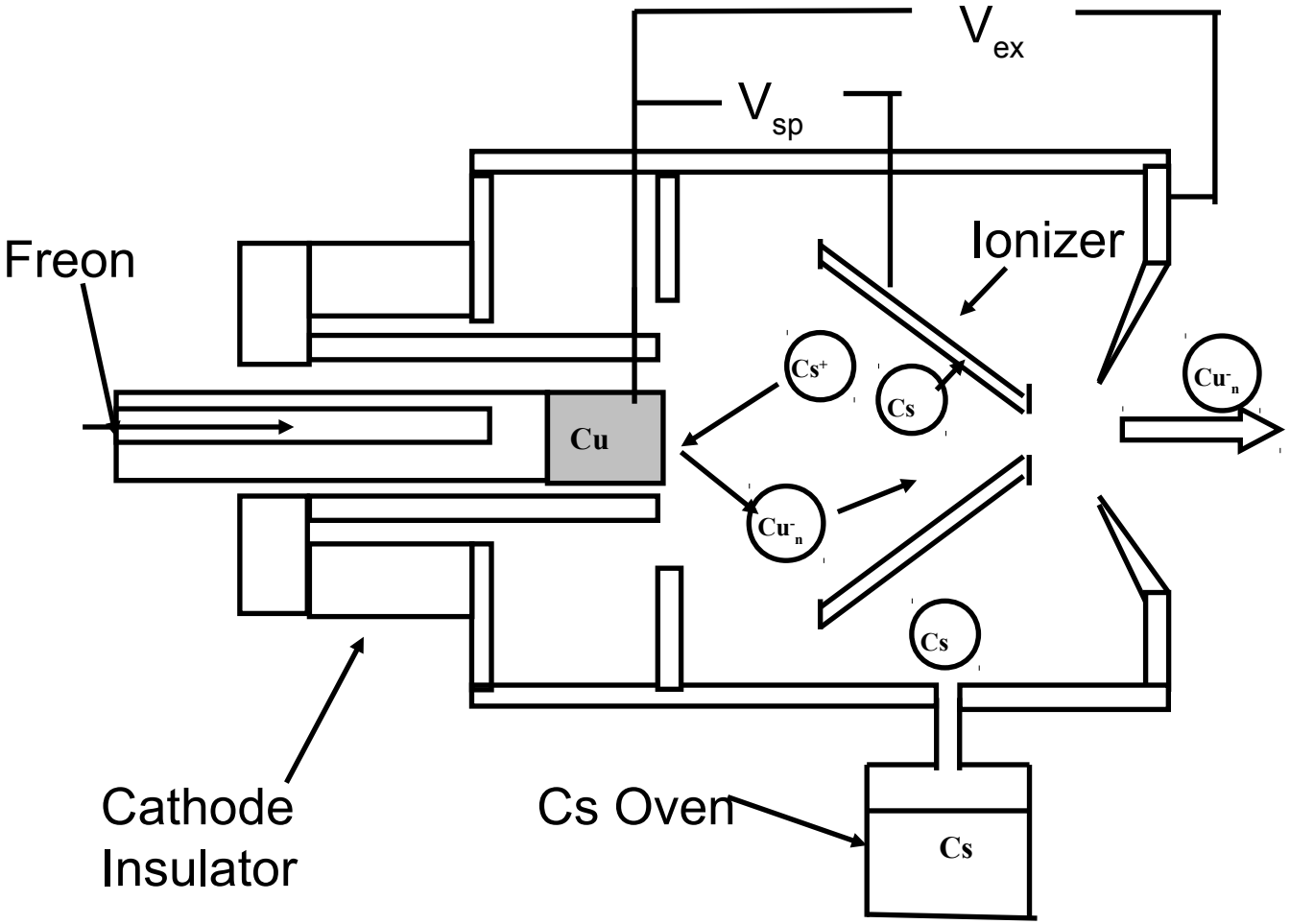
Ion Imaging

- Obtained by using
  - Ion Microscope [Resolution : 2-5μm]
  - Ion Microprobe [Resolution : 0.5-1μm]



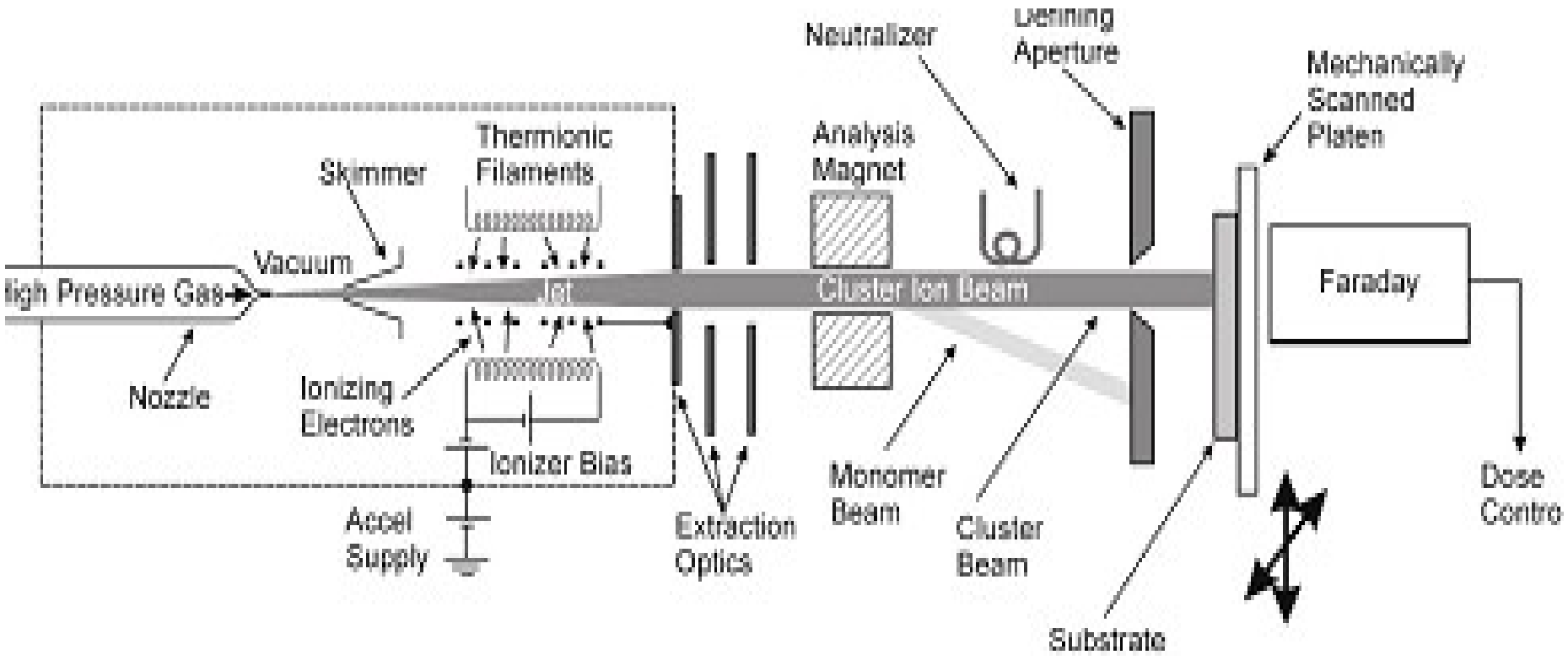
The (microprobe) images show a pyrite (FeS_2) grain from a sample of gold ore with gold located in the rims of the pyrite grains. The image on the right is ^{34}S and the left is ^{197}Au. The numerical scales and the associated colors represent different ranges of secondary ion intensities per pixel

Source of Negative Ion Cesium Sputtering (SNICS)

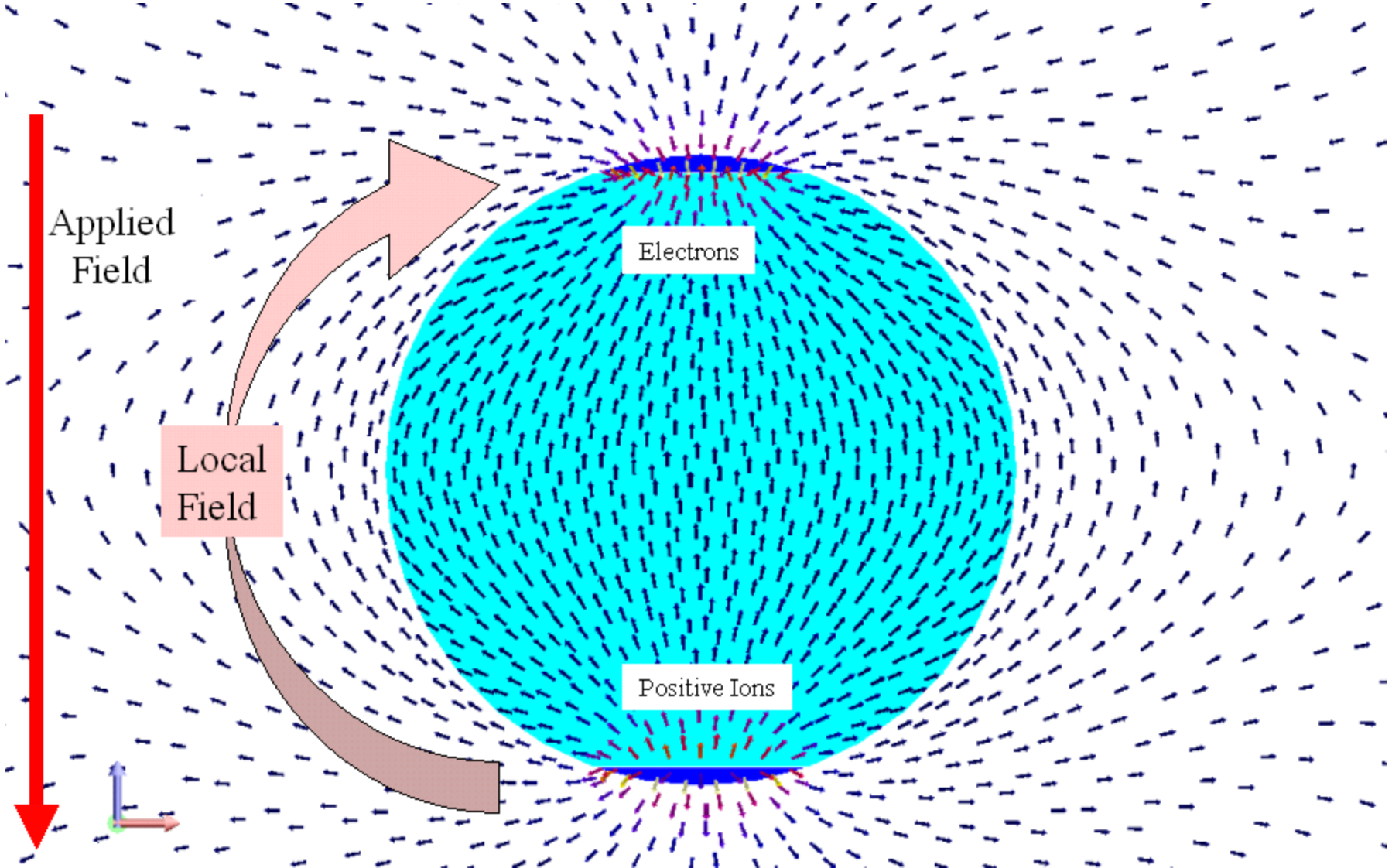



DANGER
DANGER
5/19/2003

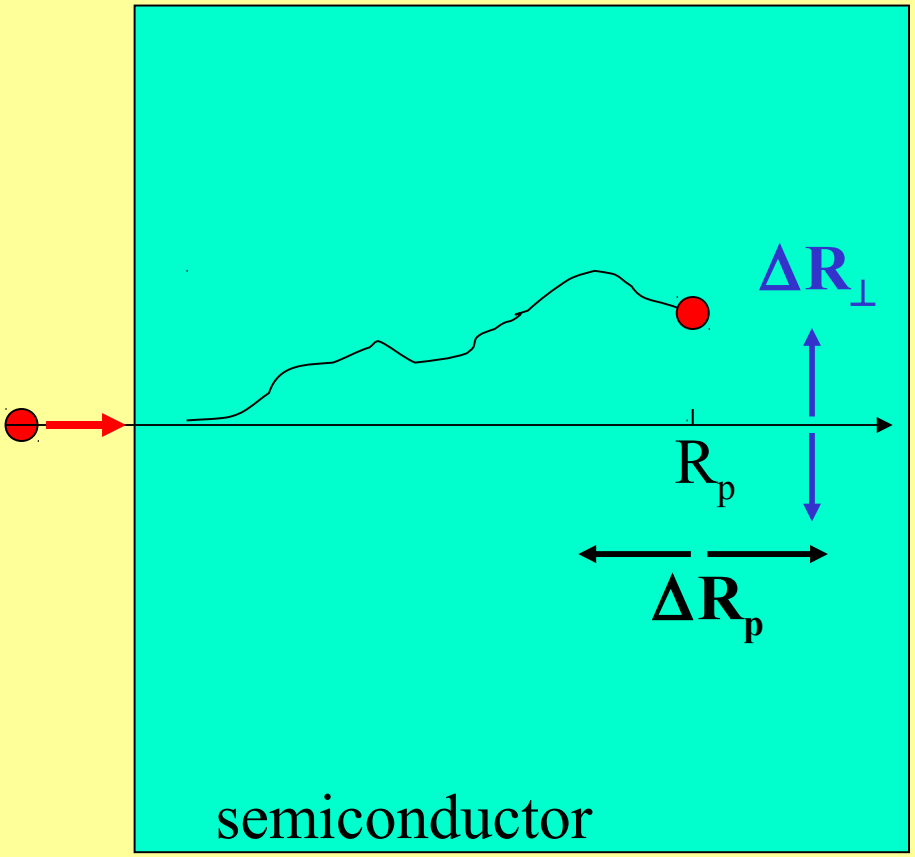
THEORY SKETCH OF THE PREVIOUS SYSTEM – easy 2 understand



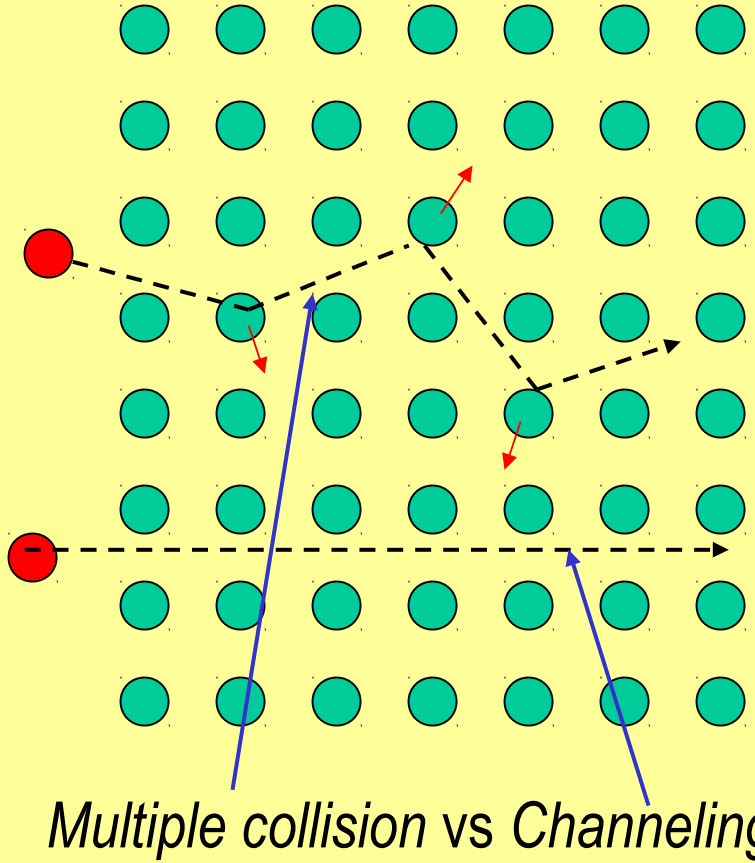
IMPACT OF ION IMPLANTATION @ ATOMIC SCALE



Ion Implantation

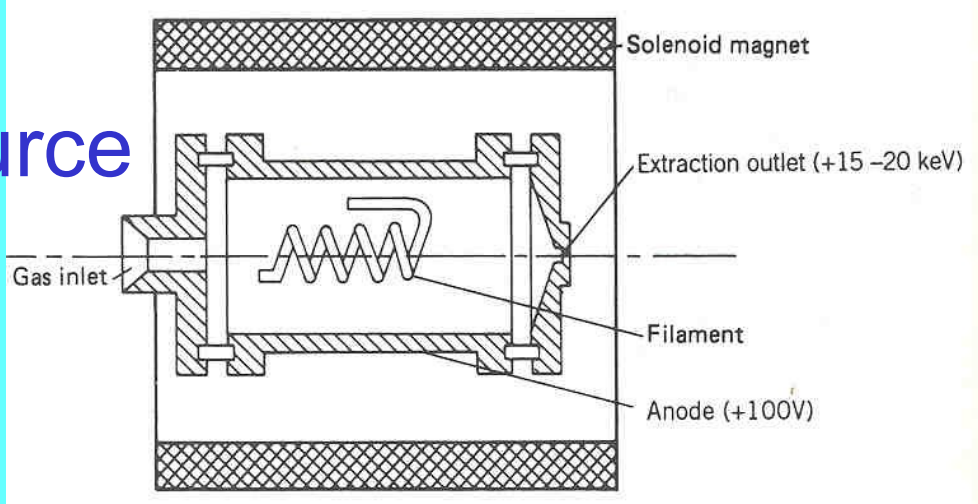


Ion trajectory, projected range & straggle

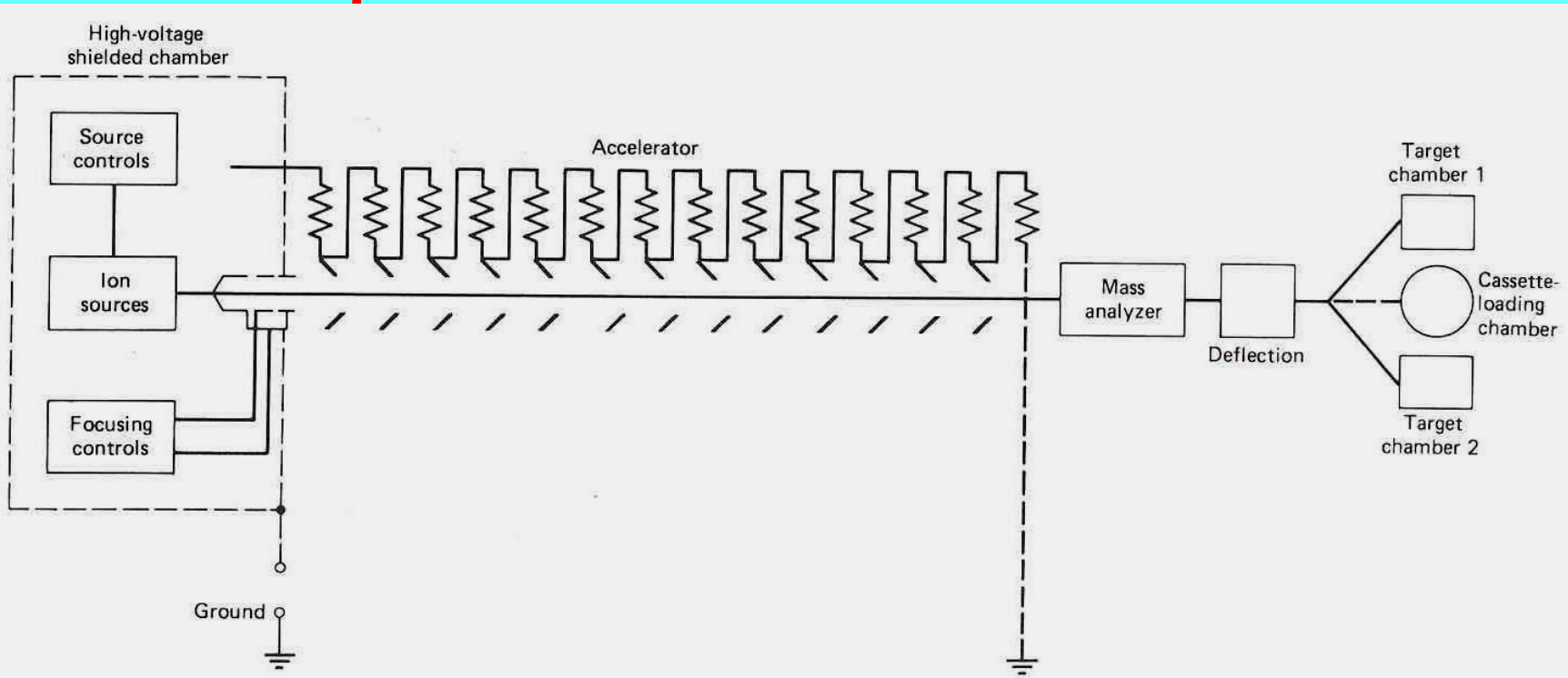


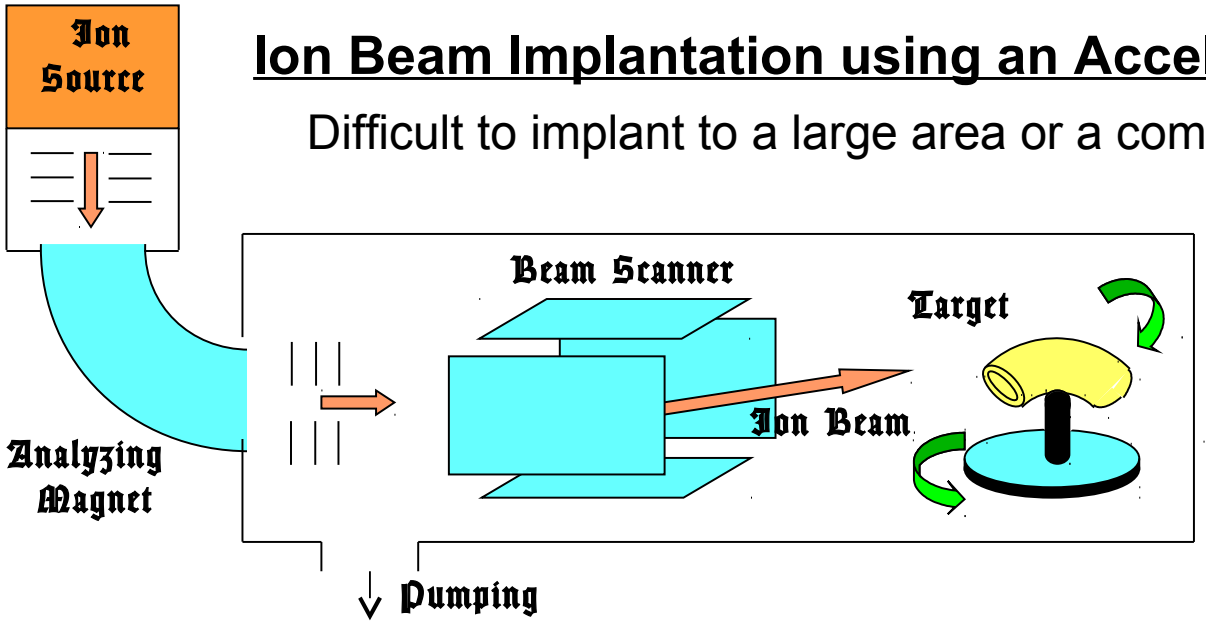
Multiple collision vs *Channeling*

Ion Source



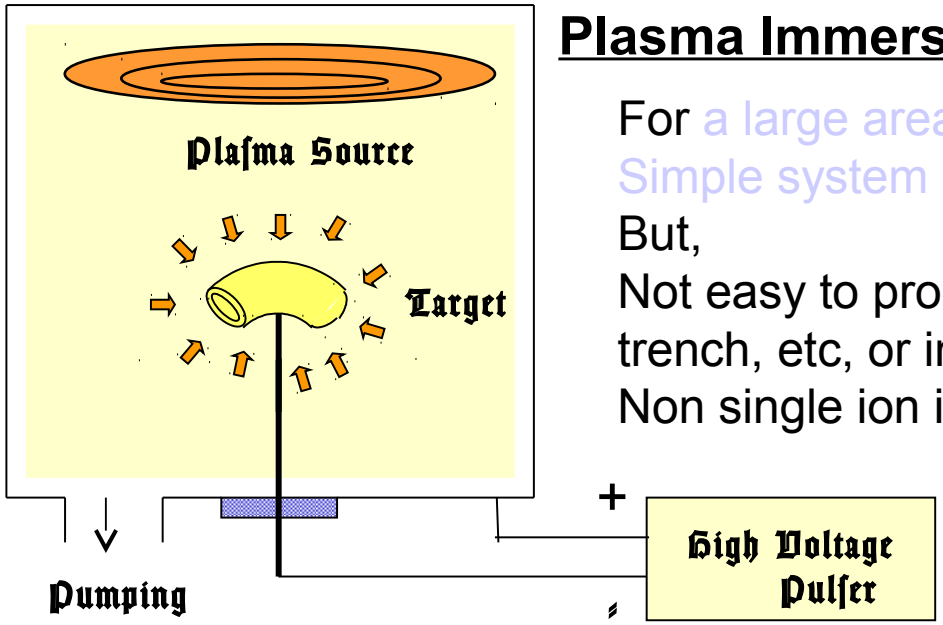
Ion Implanter





Ion Beam Implantation using an Accelerator

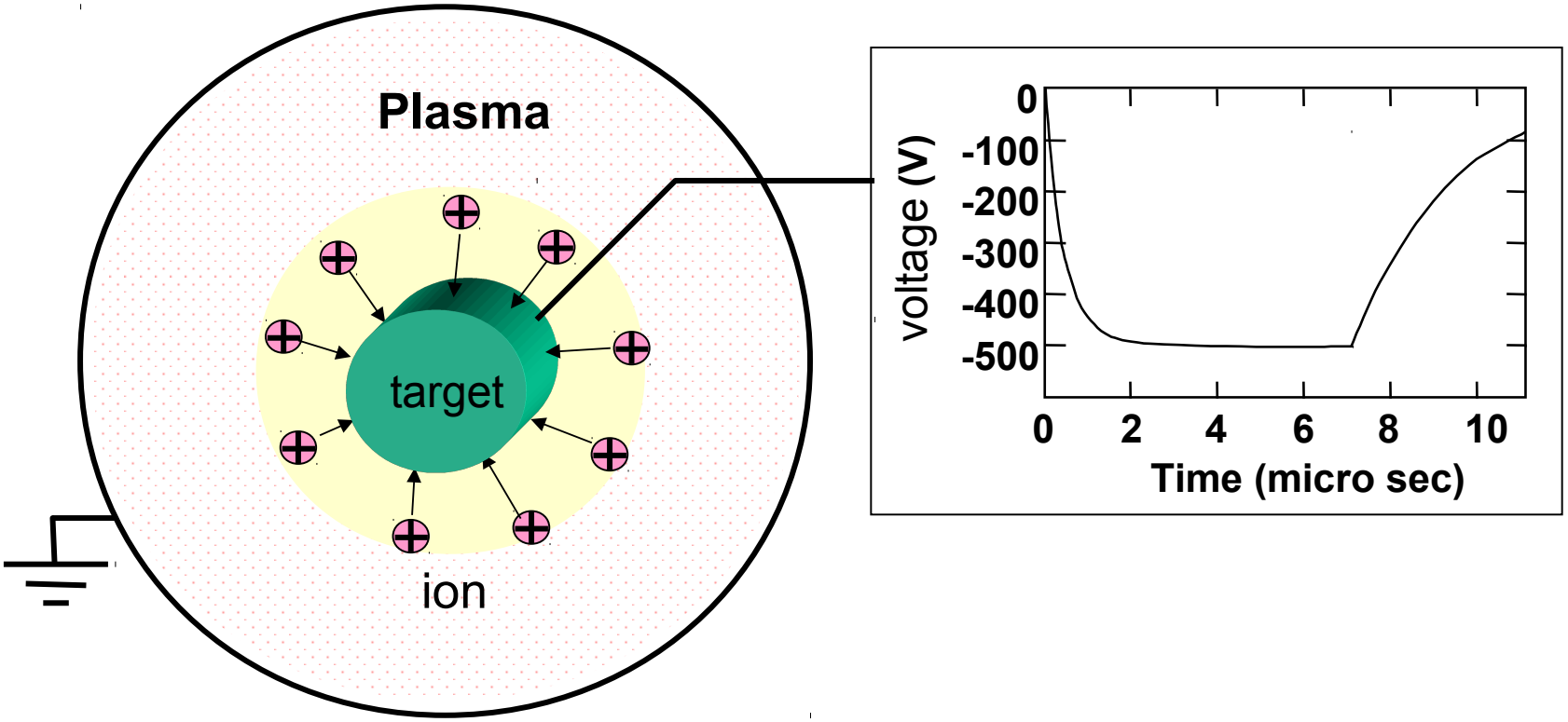
Difficult to implant to a large area or a complicated shaped target



Plasma Immersed Ion Implantation (PBII, PIII)

For a large area or a complicated shape target.
Simple system structure is another good point.
But,
Not easy to process the target with a narrow hole, trench, etc, or inside of a pipe.
Non single ion implantation is another demerit

Plasma Immersed Ion Implantation



When a pulsed negative high voltage (V) is applied to the target which is immersed in a plasma, an ion sheath is formed around the target.

The potential of the plasma is about a few ten voltage, so, ions are implanted from the sheath edge to the target.

Ion Implantation of Dopants

- One way to reduce the spreading found with diffusion is to use ion implantation
  - also gives better uniformity of dopant
  - yields faster devices
  - lower temperature process
- Ions are accelerated from 5 Kev to 10 Mev and directed at silicon
  - higher energy gives greater depth penetration
  - total dose is measured by flux
    - number of ions per cm^2
    - typically 10^{12} per cm^2 - 10^{16} per cm^2
- Flux is over entire surface of silicon
  - use masks to cover areas where implantation is not wanted
- Heat afterward to work into crystal lattice

Applications of Ion Implantation

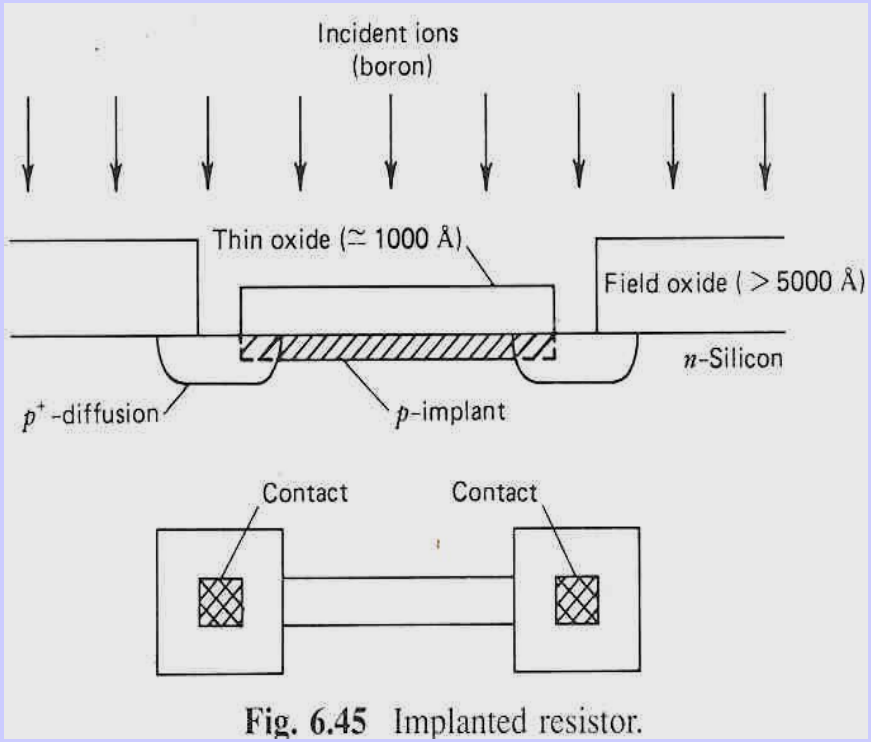


Fig. 6.45 Implanted resistor.

Resistor

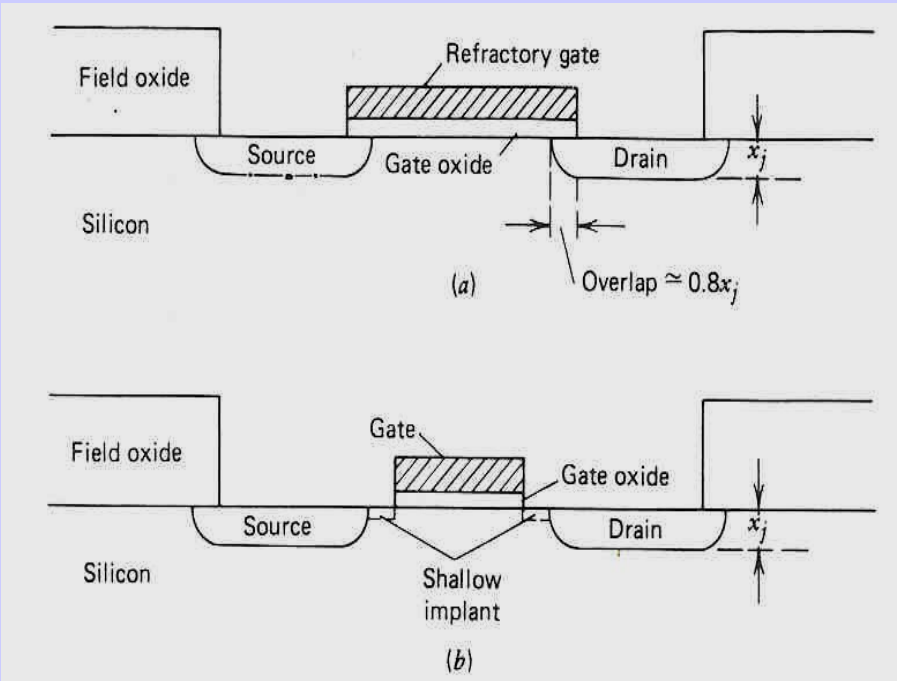


Fig. 6.47 High-speed MOS device using ion implantation.

High-speed MOSFET

ANALYSIS OF FAILURE MODEL

- VERIFICATION
- DETECTION
- HEALING

Reliability Test:

Data Retention and Endurance Test Results

Test time in hours:	168hr	500hr	686hr	1000hr	1168hr
1) Program devices and soak @ 200C	231/ 0	231/ 0			
2) Prog. 10,000 times @ 70C		231/ 0			
3) Program (inverse pattern); soak @ 200C			231/ 0	231/ 0	
4) Program (non-inverse pattern), soak @ 200C					231/ 0

No test failures were recorded during the above tests.

(Note: values are: sample size/ # of failures)

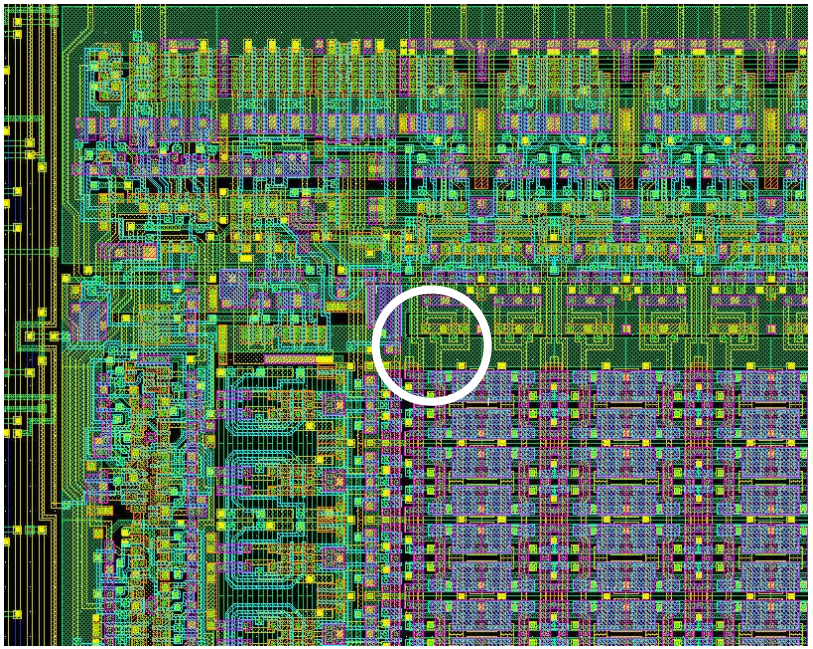
Failure Rate Calculation:

Data Retention Life Testing for C7:			
Experiment parameters:			
Confidence Level:	90%		Calculation is based on Arrhenius model for thermally activated failure mechanisms.
Test temperature °C:	200		
Duration in hours:	1168		
Chi-squared Factor:	4.605		
Sample size:	231		
Number of failures:	0		
Activation Energy in eV	0.7		
Avg. use temp.°C	55		
Results:			
Acceleration Factor:	1982.924492		
MTBF (low limit) in hours	117180.456		
MTBF in hours	232359996.2		
FAILURE RATE (FIT)	4		

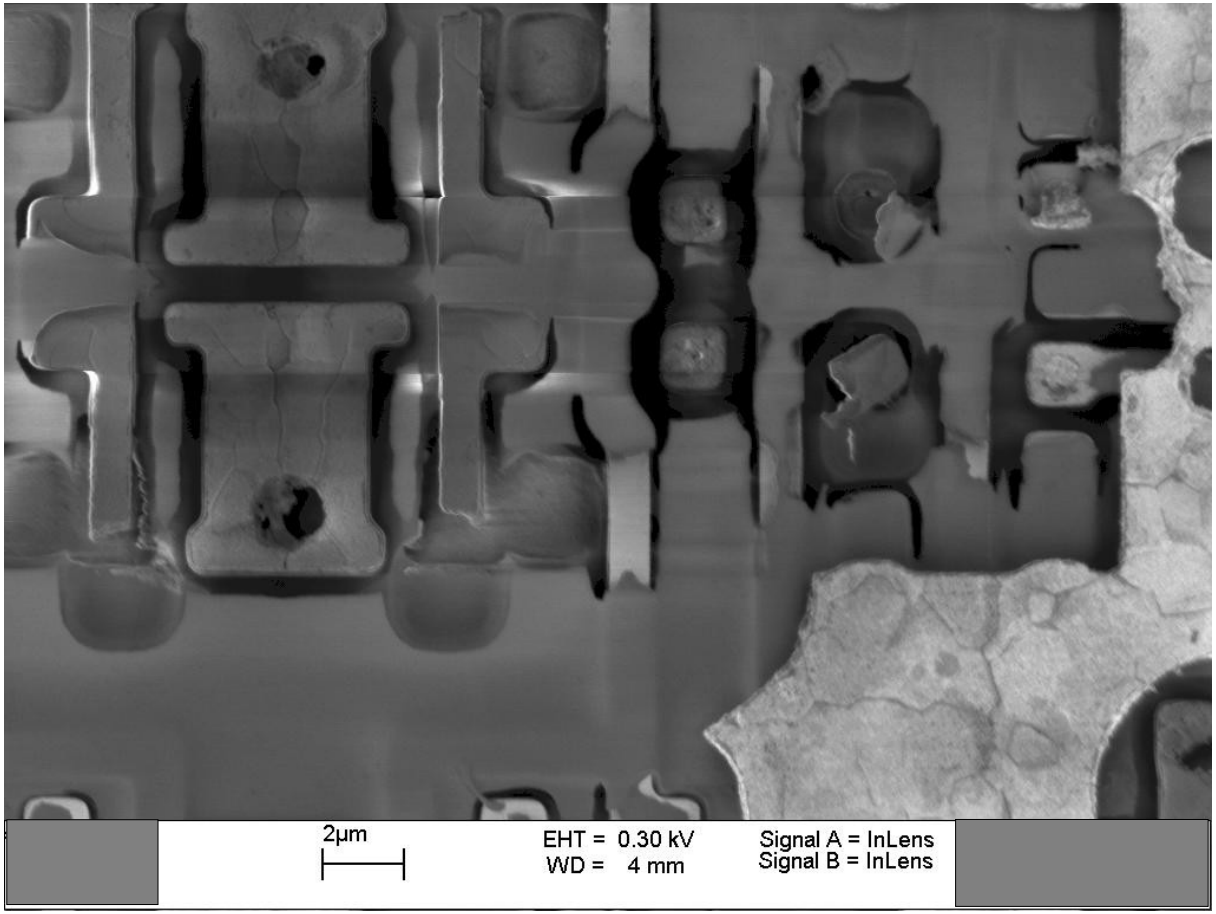
Note: 3 lots of 77 pcs. tested

Failure Analysis steps:

- Application of high temperature stress resulted in a change to the trip point temperature. So the cell was still leaking and was sensitive to thermal stress. Corner cell of the matrix.
- Time to "peel back the onion"…

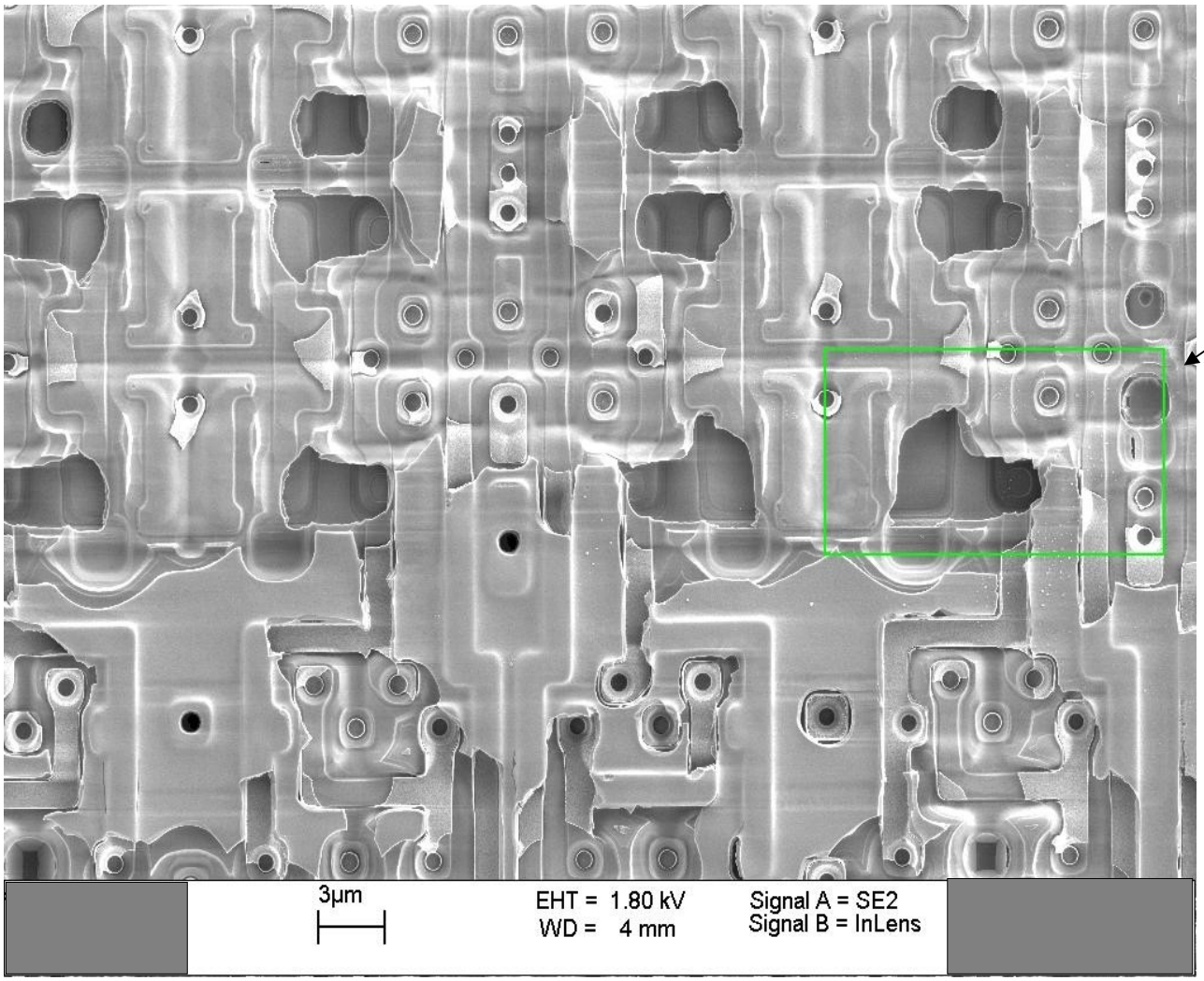


Failure Analysis steps:



Potential voltage contrast (PVC) image of layer 1 metal

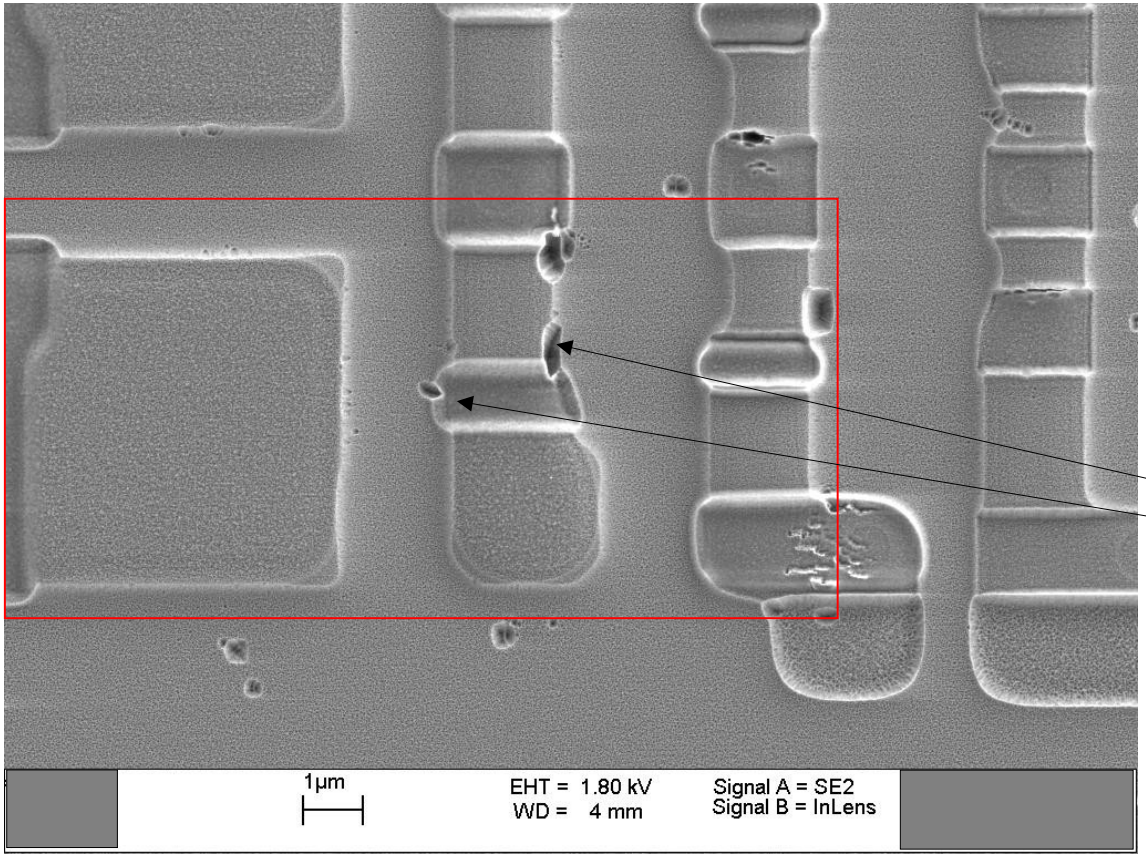
Failure Analysis images:



SEM picture with marked failed cell (circled in green). Note layer 1 metal is removed.

Failure Analysis images:

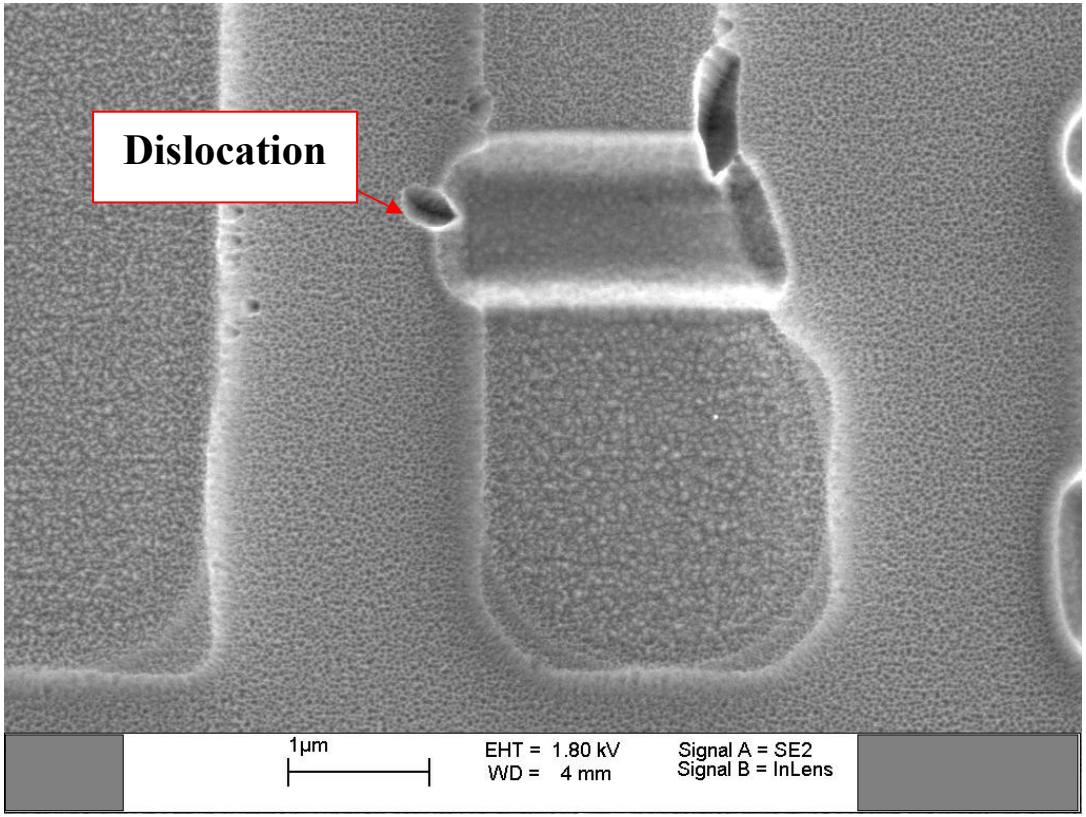
SEM picture of the complete failed cell after 30 s Wright etch



Dislocations

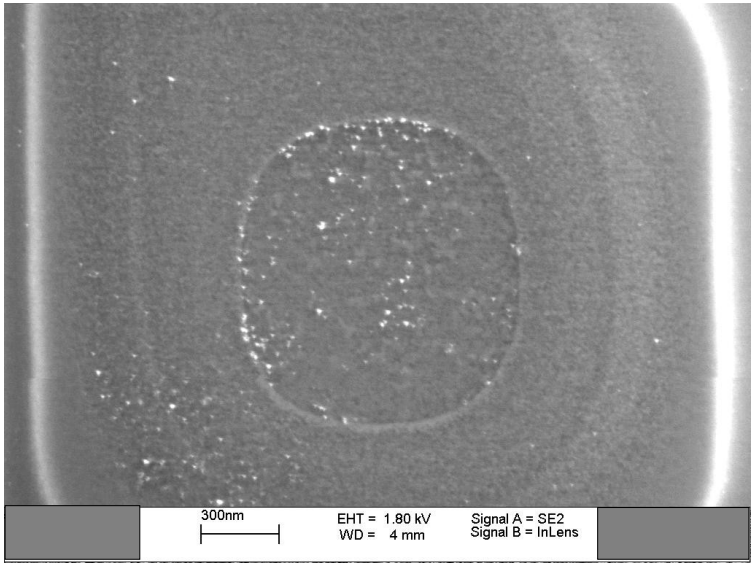
Failure Analysis images:

Higher magnification

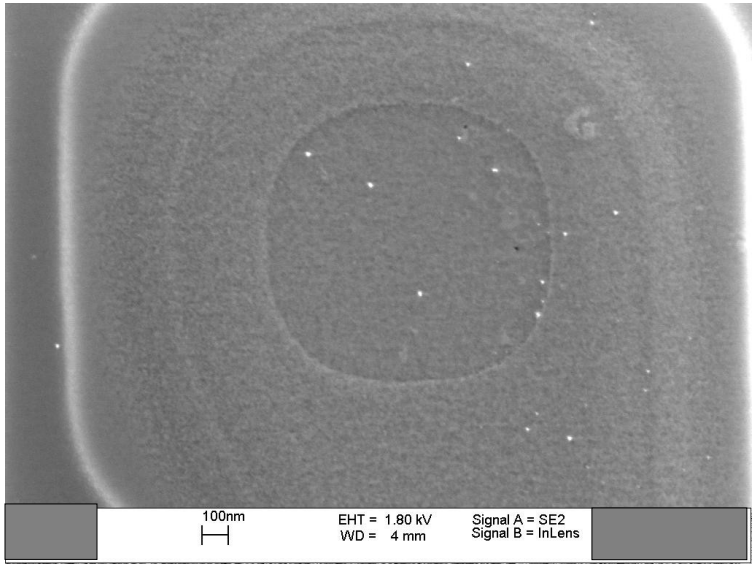


Failure Analysis images:

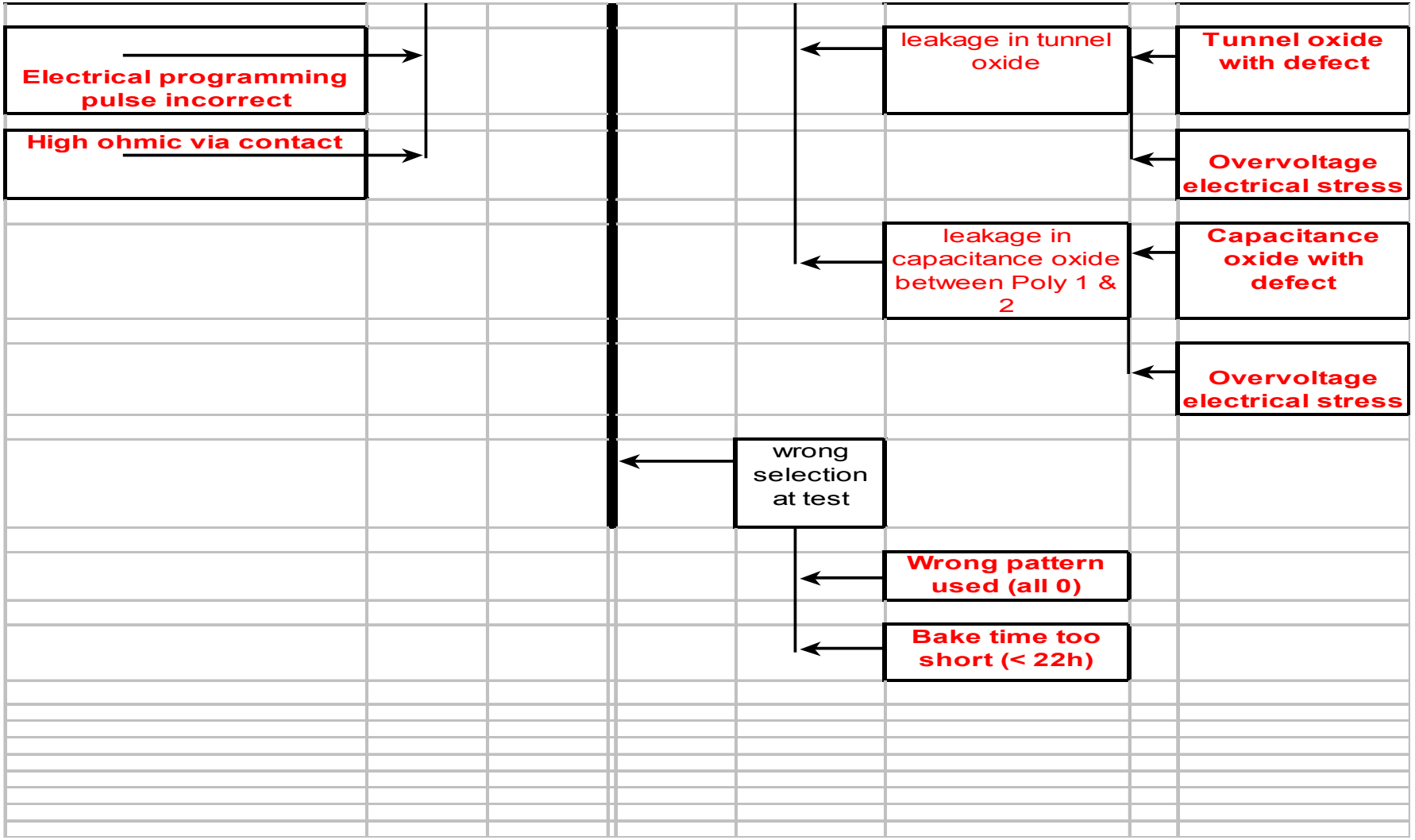
SEM image of the tunnel window of the failed cell with the tunnel oxide is removed (high magnification)



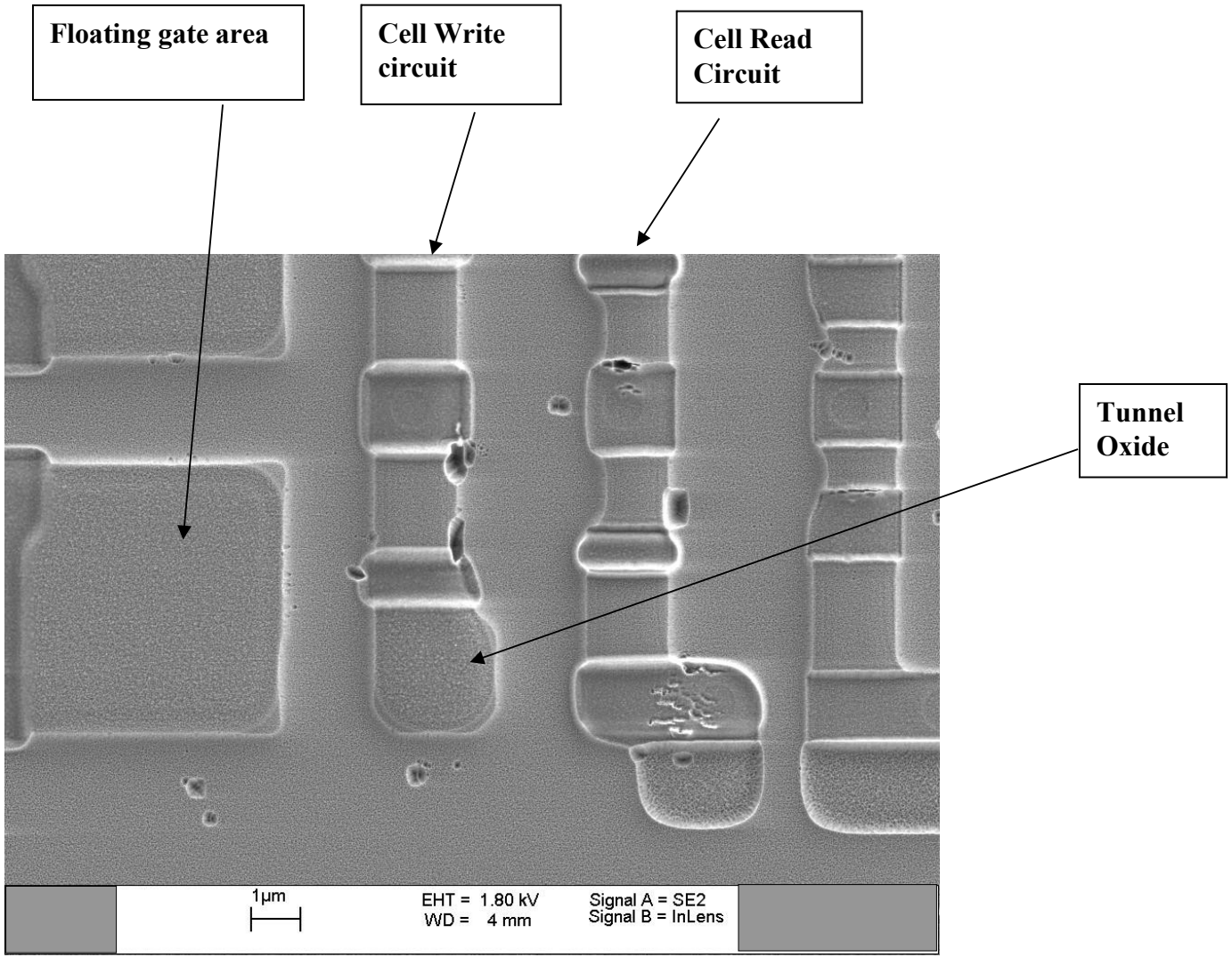
SEM image of a tunnel window in the neighborhood cells



Ishikawa / Fishbone Diagram:

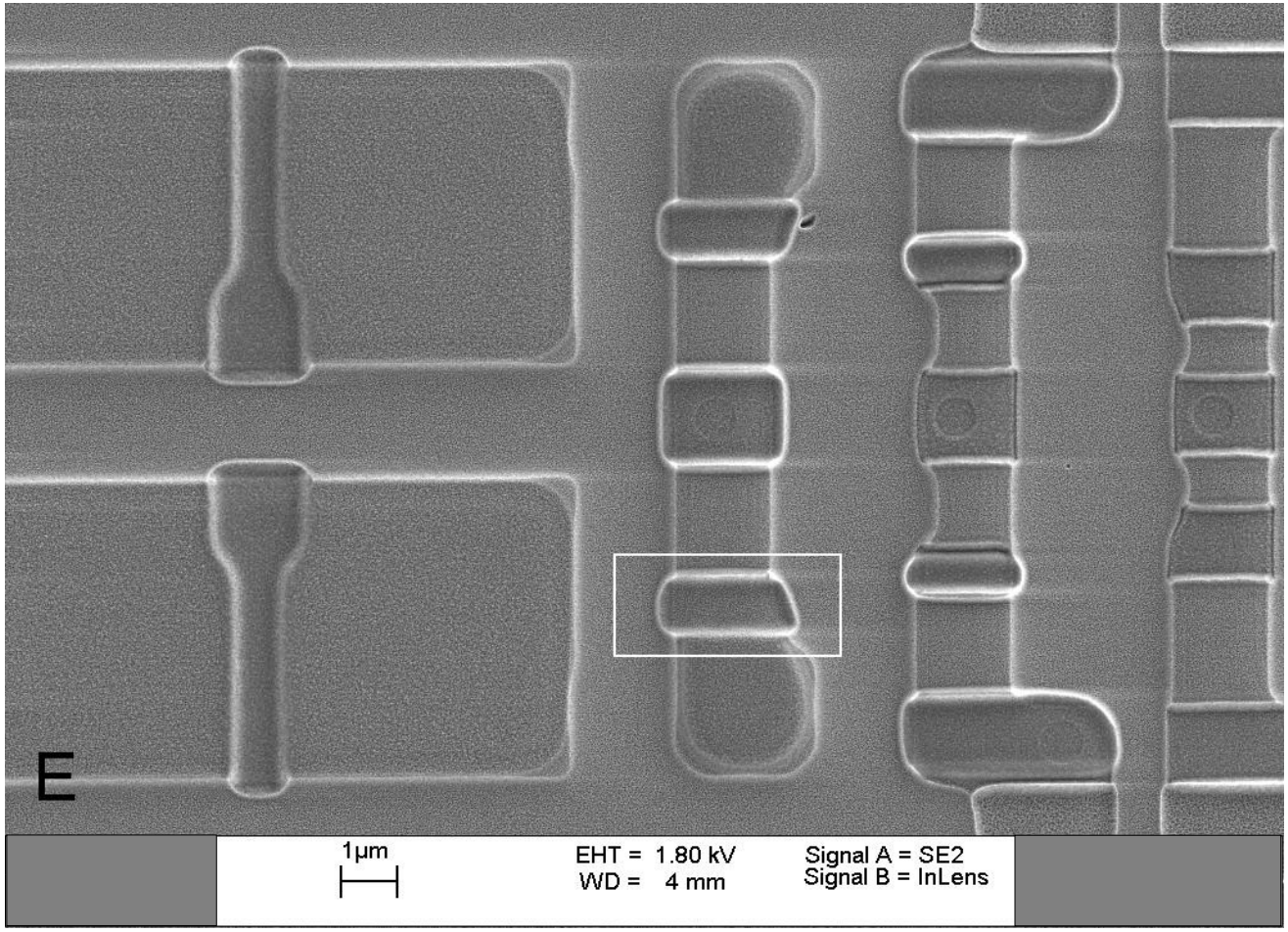


Failure Analysis images:

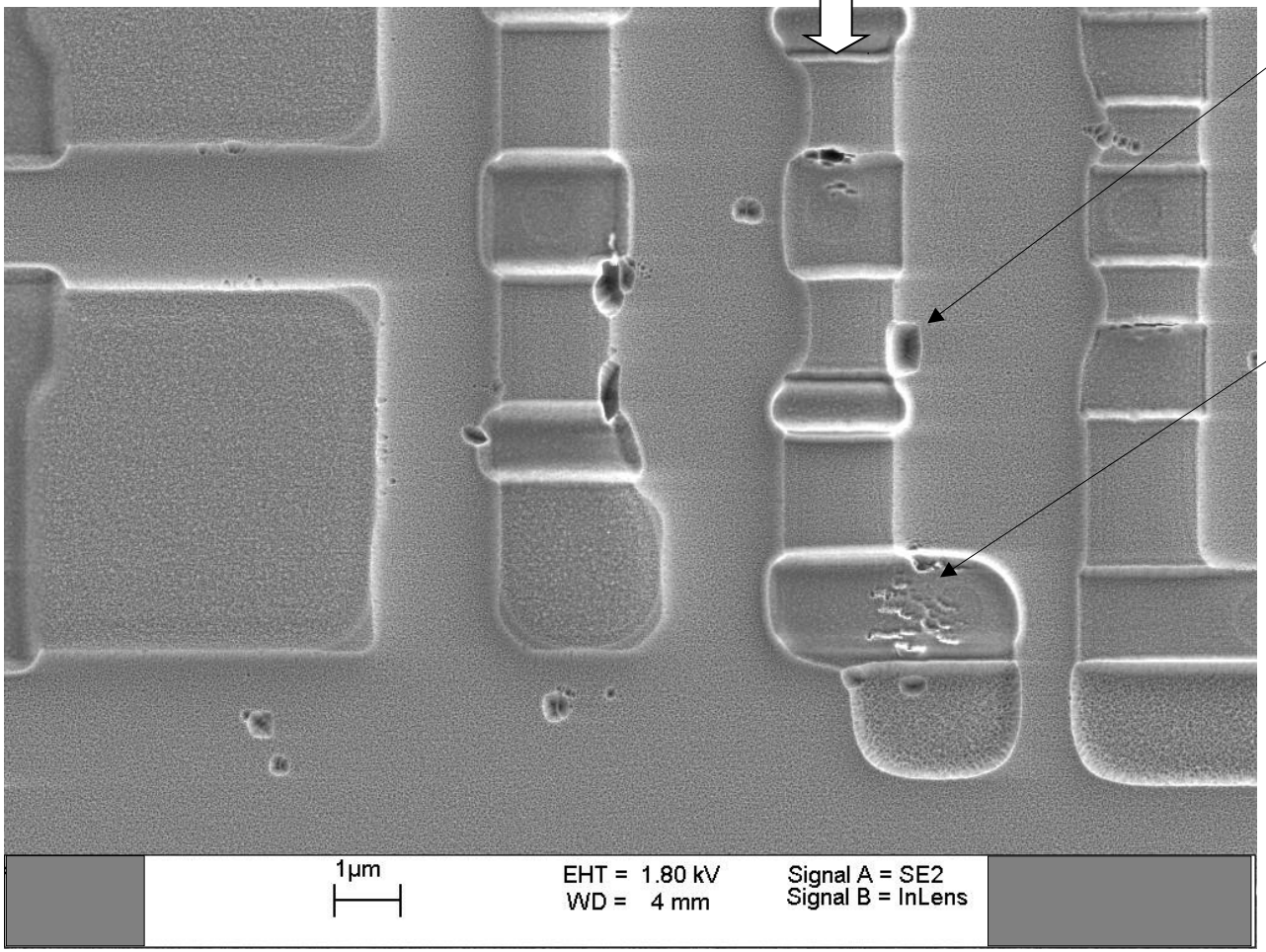


Failure Analysis images:

Backpreparation of this device from customer that passed all testing. Each device shows a low density of dislocations in the key active circuit area. Note that some small amount of dislocations is normal.



Failure Mechanism found !



Pit caused by electrical overstress.
May have started out as a dislocation.

Region damaged by electrical overstress; the area was altered by current to ground.

Failure Mechanism:

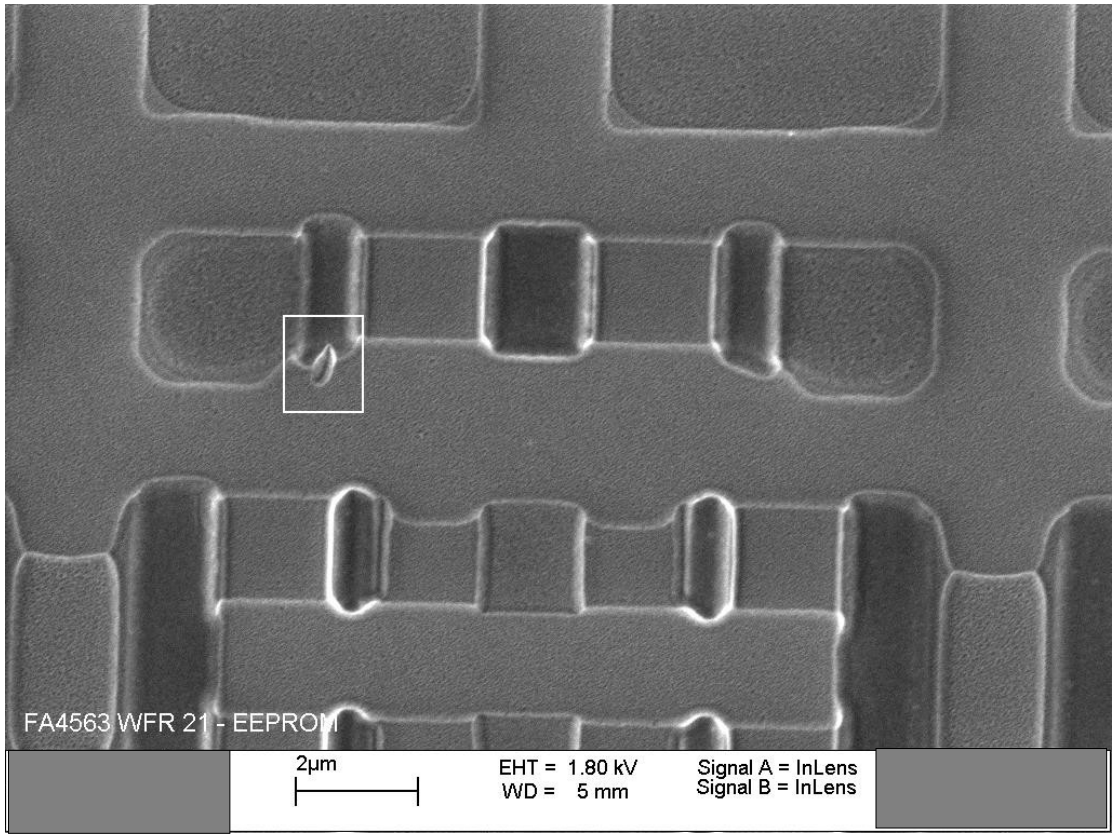
- The failure mechanism for the single bit failure was caused by electrical overstress (EOS) in the bit line circuitry at the read select transistor of the floating gate cell.
- There is physical evidence of this EOS damage; see prior photograph. The added resistance from the Gate to Drain on the select transistor caused the "1" to be read as a "0" since it creates a voltage divider with the Drain to Source impedance.
- Probable failure mode is that a silicon defect transformed into an EOS site after thermal shock test resulting in the changed circuit characteristic.

Corrective actions:

- ZMD would like to reduce the defect density of dislocations. A separate DOE effort is planned and will improve the reliability and yield of all ZMD IC products.
- The containment of similar single bit errors is best done using a rigorous wafer level screen. Increasing the endurance programming operating temperature (coupled with high voltage) will aid the detection of defect leakage currents if they are present.
- Additional writing all 0’s to the EEPROM after the checkerboard tests will assure that the EEPROM cells are capable of this stringent condition.

Results:

Specific types of dislocations were created when 3 process factors were varied in the experiment… but higher thermal annealing temperature can reduce occurrence of dislocations.



References

- http://www.play-hookey.com/semiconductors/pn_junction.html
- http://rel.intersil.com/docs/lexicon/manufacture.html

In the hope that we may slay the dragon!

Thank you for your interest and attention.

Conclusion