INVITED PAPER

Silicon Crystal Growth and Wafer Technologies

This paper reviews the historical development of semiconductor silicon wafer technology including recent advances in wafering and bulk crystal growth, and discusses technologies that will take us beyond current CMOS capabilities.

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ABSTRACT | Silicon substrates form the foundation of modern microelectronics. Whereas the first 50 years of silicon wafer technology were primarily driven by the microelectronics industry, applications in photovoltaics (PV) also promise to drive new advances in silicon wafer technology over the next ten years. In the first part, we review the historical development of semiconductor silicon wafer technology and highlight recent technical advances in bulk crystal growth and wafering technologies, including the development of silicon-on-insulator (SOI) technologies and ultrathin wafers. We then discuss technologies that could take us beyond the current capabilities of complementary metal–oxide–semiconductor (CMOS) devices. In the second part, we review silicon manufacturing for PV applications and some unique wafering technology challenges in that field. Finally, we summarize industry roadmaps and product needs highlighting key technical areas which promise to shape the future of silicon wafer technologies in the coming decades.

KEYWORDS | Photovoltaics (PV); semiconductor materials; silicon; substrates

I. INTRODUCTION

Silicon accounts for well over 90% of all semiconductor and solar cell wafer production. During the early days of semiconductor electronics, discrete transistors were typically made from germanium. The lower melting point of germanium meant that crystals were easier to grow. However, this did not last long and the lighter, cheaper, stronger, more abundant element silicon was soon a contender for transistor production. By the late 1960s, at the start of the integrated circuits industry, silicon was favored for two main reasons. First, silicon has a larger bandgap giving it the ability to operate at higher temperatures (see Table 1), and second, because of the remarkable synergy with its oxide, silicon dioxide (SiO_2, quartz glass). By simply heating silicon in an oxygen containing atmosphere, a high dielectric strength, electrically insulating SiO_2 layer is inexpensively formed. This SiO_2 layer is chemically and mechanically very stable, effectively passivates the surface states of the underlying silicon, forms an effective diffusion barrier for the commonly used dopant species, and can be easily preferentially etched from the silicon, and *vice versa*, with high selectivity. By contrast, GeO_2 is a chemically unstable, poor electrical insulator that is 33 times more soluble in water than SiO_2, making it less suited to the photolithographic and wet chemical processes used to fabricate integrated circuits.

Table 1 Maximum Operating Temperature for Various Semiconductors. Commercial Device Specifications Are Significantly Below These Ratings

Material	Bandgap @ T_{room} (eV)	Approx T_{device} (°C)
Ge	0.67	100
Si	1.1	250
GaAs	1.42	400
GaP	2.26	800
β-SiC	2.2	800
α-SiC	3.1	~1000
GaN	3.4	~1000

Silicon semiconductor material has been studied for over 50 years and the silicon wafer industry today now has

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the advantage of a wide ranging infrastructure. The vast body of science and engineering development that has gone into silicon makes it the most studied element on earth. It is known how to cut, etch, lap, grind, polish, and clean silicon in more ways and in more detail than for any other material. The advantages of silicon relative to other material choices for electronic devices are clear. Its abundance and the wealth of knowledge about how to process it make it among the lowest cost contenders. The remarkable combination of high-quality semiconductor and high-quality insulator embodied in the Si/SiO_2 material system is nearly unique among semiconducting materials and is in large part responsible for the astonishing progress in semiconductor devices over the past half century. In terms of performance, speed and power dissipation are adequate for most devices, and although some other materials may exceed silicon's performance for some specific parameters, these market sectors tend to be relatively small and specialized leaving silicon the optimum choice for the vast majority of devices. In 2010, the production and sale of semiconductor silicon wafers was a $10 billion industry feeding a $314 billion device industry and that, in turn, supplied an electronics market worth over $1.2 trillion. Solar applications involving both single and multicrystalline silicon added a further $5 billion to wafer sales.

Even so, progress in semiconductor device design is pushing silicon to its performance limits. In the last several years, it has become clear that traditional scaling of gate length and gate oxide thickness will no longer return the same gains in transistor performance as in past generations [1]. Issues with active power dissipation during transistor switching, high leakage currents in the transistor off-state, and short channel transistor effects have become major barriers to aggressively scaled complementary metal–oxide–semiconductor (CMOS) transistors. High-power/high-voltage devices need progressively lower resistivity silicon substrates to function efficiently, and eventually may migrate to higher band gap materials like gallium nitride (GaN) grown on silicon in order to overcome silicon limits for on-resistance and breakdown voltage [2]. Further, as silicon is pushed into radio-frequency (RF) operating ranges, higher resistivity substrates are needed to isolate transistors and passive components. As chip performance requirements advance, solutions to these problems differ widely and, necessarily, we see new device architectures and the introduction of new materials. New materials such as Cu metallization, SiGe source/drain, and the high K/metal gate replacement for silicon dioxide have been successfully integrated with silicon at the device fabrication level in order to overcome transistor scaling limitations. Even with new materials integration, silicon remains the substrate platform on which advanced integrated circuits and power devices will continue to be fabricated.

In the last decade, solar applications of silicon have become more significant in terms of the volume of silicon used. Around 2006, the mass of silicon used by the solar industry surpassed that used by the semiconductor industry for the first time. In 2010, of the estimated 160 kT of electronic grade polysilicon production, over 80% was consumed by the solar industry.

We review the progress made by the silicon wafer industry in keeping up with the progressions of Moore's law and the increasing demands of the solar industry, and discuss the prospects for various silicon substrate technologies over the coming decade or more.

II. SILICON SUBSTRATE MATERIALS TECHNOLOGY

In the 1950s, crystals were grown mostly by the float zone (FZ) process and wafers were etched after diamond polishing to remove microscratches, but in the 1960s, much of the fundamental work for the current silicon industry was initiated. Although the basic silicon process has remained largely the same since that time, the industry has provided a steady stream of incremental, but nevertheless significant improvements in capability to produce large, flat, clean surfaces of silicon at lower cost. Commercially available epitaxial and silicon-on-insulator (SOI) wafers are commonplace and wafer diameters have increased from 0.5 in to 300 mm in production and 450 mm is now in the research and development phase [3]. Similarly, crystal growth and substrate technologies are rapidly evolving to become a specialty manufacturing platform that can address the unique needs of the solar industry [4].

While fundamental processes in the manufacturing of silicon wafers have been in place for quite some time, silicon manufacturing technology has continuously improved in order to meet the silicon wafer parametric capability and cost requirements necessary to sustain scaling progress on semiconductor and solar industry roadmaps. Manufacturing methods commonly used in the industry are outlined in Fig. 1 and the key aspects for various processes are described in the following sections.

A. Production of Polysilicon

Silicon is the second most abundant element in earth's crust, in the form of silica (SiO_2) and silicates, and is readily extracted from silica-rich sands. In nature, it typically contains large amounts of impurities and so the initial stages of the manufacturing process are concerned with reduction and purification of the silica sand to produce metallurgical grade polysilicon, typically $> 98\%$ pure silicon. This is then further refined to produce solar and semiconductor grade polysilicon, which can be used as the feedstock for crystal growth to produce semiconductor grade single crystal silicon suitable for device manufacturing. Generic processes for the purification of silicon and the manufacture of silicon crystal and wafers are well established.

Metallurgical grade polysilicon (MG) is produced through the reduction of silica by mixing it with carbon and heating, typically in an electric arc furnace, to over

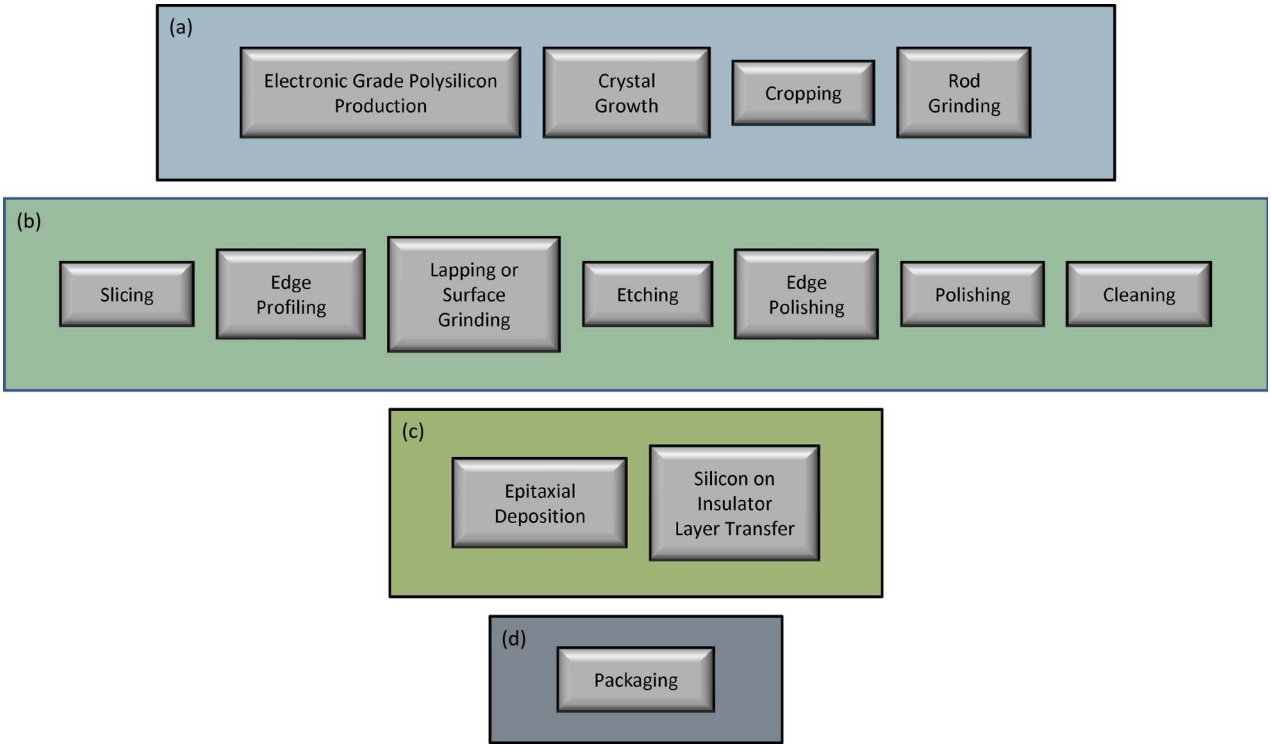


Fig. 1. ***Typical silicon industry production processes. (a) Ingot production. (b) Wafering processes. (c) Optional processes for advanced products. (d) Final product packaging and shipping.***

1900 °C. Silicon produced by this method typically contains ∼2% impurities although this may be reduced somewhat through the use of higher purity silica and carbon feed materials.

The most commonly used process for further purification to electronic grade silicon converts the metallurgical grade material to trichlorosilane (TCS), which is in liquid form and easily purified through subsequent distillation

$$\mathrm{Si(MG)} + 3\mathrm{HCl} \rightarrow \mathrm{SiHCl_3} + \mathrm{H_2}.$$

This typically takes place in a fluidized bed reactor at about 300 °C. The boiling point of TCS is 31.8 °C and it is easily distilled to produce a very high purity liquid. The liquid TCS is then commonly converted to solid polysilicon by the Siemens process [5], shown in Fig. 2, in which it is passed through a chemical vapor deposition (CVD) reactor together with hydrogen at a temperature in the region of 1000 °C–1200 °C. The TCS decomposes, depositing silicon onto thin, high purity silicon rods (known as "slim rods") placed in the reactor, resulting in electronic grade (EG) polysilicon

$$\mathrm{SiHCl_3} + \mathrm{H_2} \rightarrow \mathrm{Si(EG)} + 3\mathrm{HCl}.$$

Other intermediate compounds such as silicon tetrachloride ($SiCl_4$) and silane (SiH_4) can also be used.

An alternative method of production involves decomposition of silane in a fluidized bed reactor (FBR) [6]

$$\mathrm{SiH_4} + \mathrm{H_2} \rightarrow \mathrm{Si(EG)} + 3\mathrm{H_2}.$$

This technique utilizes heated silane and hydrogen gases, which are injected into the bottom of the reactor causing a bed of small silicon seed granules to become fluidized. The silane decomposes in the hot reactor and silicon is deposited on the seeds causing them to grow in size and weight. Once grown to the desired size, the granules (Fig. 3) are extracted from the bottom of the reactor while fresh seed particles are fed into the top of the reactor. Fluidized bed reactors utilize nearly all the silane gas fed into the reactor, provide superior heat and mass transfer characteristics, and are energy efficient. As highlighted in Fig. 4, FBR process is also a continuous process while the Siemens process is a batch process. Thus, the FBR process is more economical than the Siemens process and is becoming more widely adopted.

Electronic grade polysilicon has impurities in the low parts per billion (ppb) range or less, a necessary requirement for production of semiconductor devices. In the solar

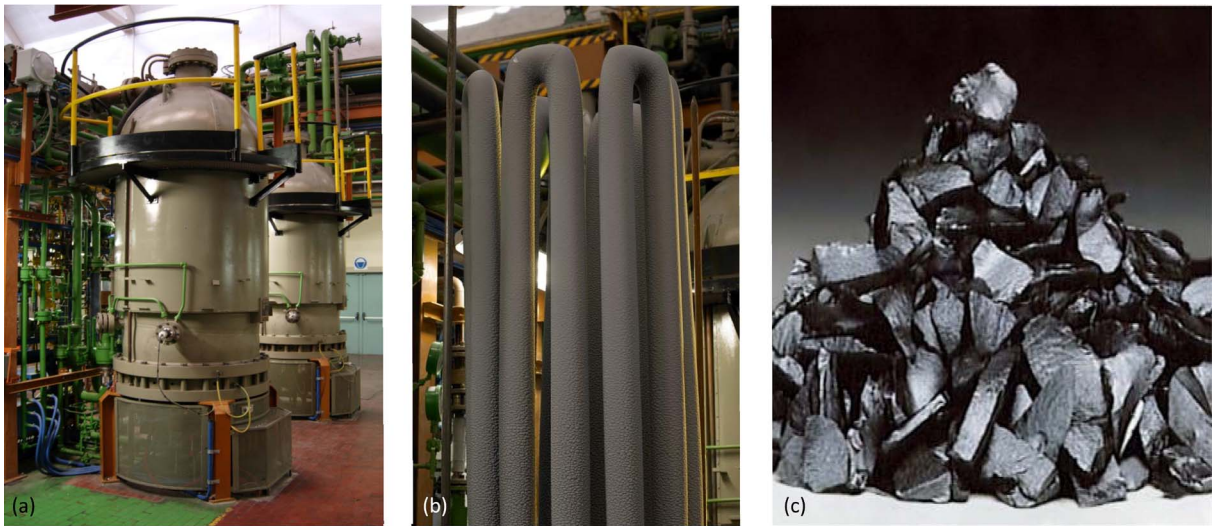


Fig. 2. *About 80% of the world's polysilicon is produced using the Siemen's process developed in the 1950s. (a) Basic Siemen's reactor. (b) As grown polysilicon rods after a reactor run. (Current generation reactors have many more rods.) (c) Final polysilicon chunks ready for loading into a crystal growth furnace.*

industry, the goal is to be able to produce energy at prices competitive with fossil fuels. To this end, solar cell manufacturers typically use solar grade silicon, which is not quite as pure but is typically cheaper. In times of shortage, market prices for silicon rise significantly and this has prompted some companies to develop "upgraded metallurgical grade" (UMG) silicon, based on alternative methods for purifying MG silicon [7]. In one such approach, impurities in MGS are removed by various hydrometallurgical processes such as acid leaching. While leaching is effective in removing impurities like Fe, Cr, Mn, Ni, and Ti, reducing phosphorus and boron to acceptable levels is particularly challenging, which impacts manufacturing yield.

B. Growth of Single Crystal Silicon

The industry standard for production of monocrystalline silicon for semiconductors is the Czochralski (CZ) method. Use of melt-based growth for semiconductor crystal growth was pioneered by Teal and Little by demonstrating the growth of single crystal Ge [8], [9]. Later, Teal and Buehler grew CZ–Si using the same technique, but they could only grow dislocated single crystals of specified orientation [10]. The first demonstration of dislocation-free CZ silicon crystal growth was demonstrated in 1959 by Dash, using a modified seeding technique [11], [12]. Growth of silicon crystals by the CZ method has been widely studied over the course of the following five decades and significant progress has been made (Fig. 5). Dislocation-free, high-purity silicon crystals

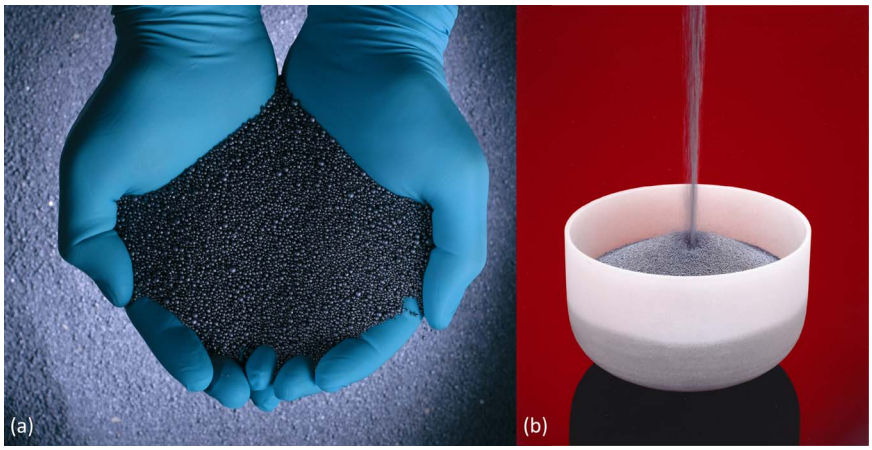


Fig. 3. *Granular polysilicon, produced in a fluidized bed reactor, has a higher packing density in the crucible and, because it flows, can be used to recharge hot crucibles which lowers cost and improves throughput of crystal growth processes.*

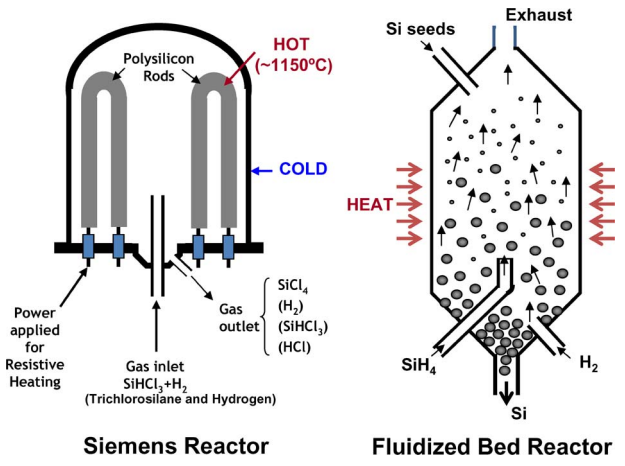


Fig. 4. *Schematic of Siemens and fluidized bed (FBR) reactors producing chunk and granular polysilicon materials, respectively. Whereas the Siemens process is a batch process, the FBR is a continuous process.*

up to 450 mm in diameter are now possible on a commercial scale.

The development of several generations of CZ single crystal pullers for growth of large crystals is shown in Fig. 6. Electronic grade polysilicon is stacked in a high-purity quartz crucible inside a crystal pulling furnace. The starting polysilicon charge, which for 300-mm crystals can weigh ~300–400 kg, is heated to a little over the melting point (1415 °C) (Fig. 7). A silicon seed crystal is dipped into the melt and slowly withdrawn at a controlled rate while the crucible and seed are slowly rotated in opposing directions. The critical variables are rates at which the crystal and crucibles are rotated and the pull rates. In the initial stages, the pull rate is quite high and the growing crystal is only about 3–4 mm in diameter. This narrow portion of the crystal is called the "neck" and was first used by Dash for producing a dislocation-free crystal and is standard practice in the industry today. In (111)- and (100)-oriented Si seed crystals, dislocations introduced due to the thermal stress of introducing the seed into the hot melt will propagate obliquely to the growth direction and will terminate on the sides of the neck rather than propagating down into the body of the growing crystal, provided the neck-length-to-diameter ratio is sufficiently large. This was an important breakthrough for the reliability of semiconductor device fabrication processes since dislocations can be killer defects in diode and transistor fabrication. Once the neck is several centimeters long, some heat is removed from the system and the pull rate is slowed allowing the crystal diameter to increase to the desired dimension. Control of pull rate (primary, fast response control) and temperature (secondary, slower response control) enables growth of large single crystals of the required diameter. At the end of crystal growth, the diameter of the crystal is tapered to form a conical tail that minimizes the number of dislocations formed by the thermal shock of withdrawing the crystal from the melt, and allows these dislocations to propagate out of the sides of the cone rather than into the body of the crystal, maintaining a dislocation-free crystal.

By the mid-1960s, dislocation-free CZ silicon crystals could be produced. Through the 1960s and 1970s, much work was done on elucidating the basic physics and materials science of the CZ silicon process. A great deal of effort was expended on identifying, characterizing, and reducing impurities in the CZ growth process, notably



Fig. 5. *Early days of Czochralski (CZ) growth crystals were small and easy to handle. Current generation crystals are large, heavy, and need specialized handling equipment.*

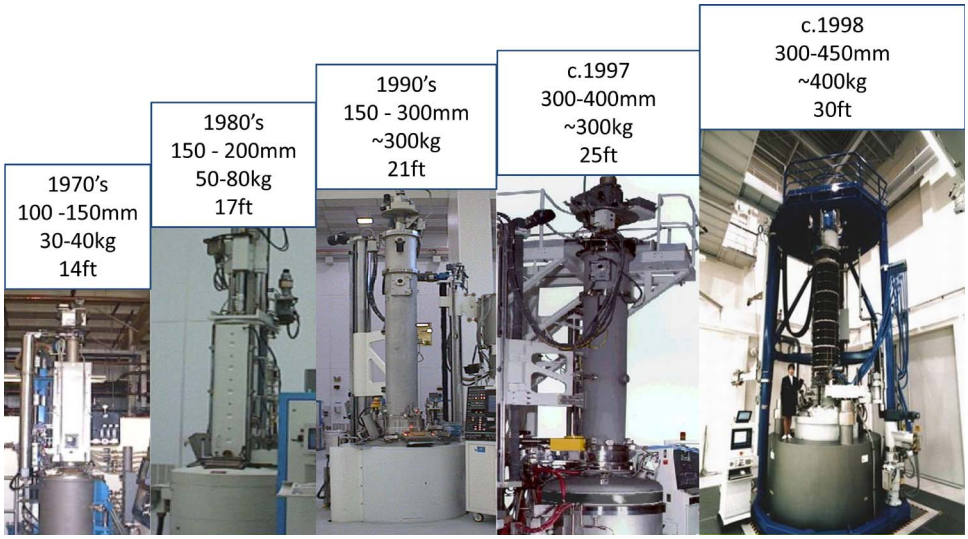


Fig. 6. *Examples of progress in Czochralski crystal pullers from 1970 through current diameter capability. Showing approximate period, crystal diameters, typical polysilicon charge weight and approximate height of the equipment above the working floor. Later models have services (water, argon, vacuum) below floor level. [Right-hand side photo shown is courtesy of Super Silicon Institute (SSI).]*

carbon, oxygen, and boron, which were at much higher levels than those of FZ silicon, and caused problems in certain device applications. With diligent effort and the advent of low boron polysilicon from the Siemens process, the impurity levels of CZ were greatly reduced, and the CZ process displaced the FZ process in all but a few specialty applications.

With impurities under control, attention in the 1980s and 1990s turned to "defect engineering" of the CZ silicon crystal, the defects referred to being oxygen precipitates and agglomerated intrinsic point defects.

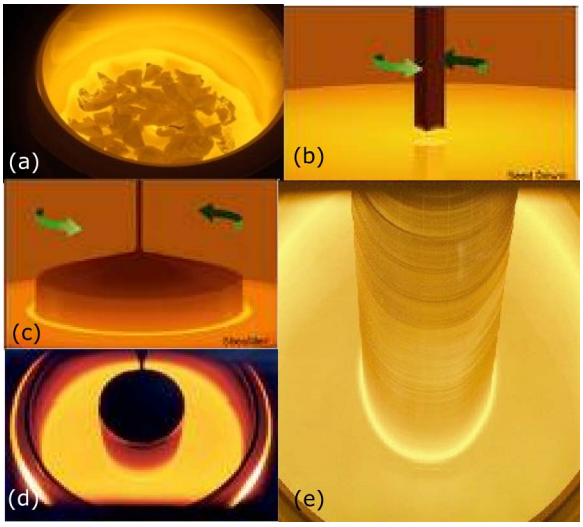


Fig. 7. *Various stages of Czochralski crystal growth: (a) meltdown; (b) seed dip; (c) top; (d) shoulder; and (e) body.*

Much of the work in the 1980s centered on understanding dissolved interstitial oxygen and its precipitation into silicon dioxide inclusions in the crystal after various thermal treatments [13]. The main contaminants in CZ silicon are the deliberately added dopant species (most commonly boron for *p*-type material and phosphorus for *n*-type material) plus interstitial oxygen atoms introduced from the slow dissolution of the quartz crucible by the silicon melt, and very small amounts of carbon introduced from the graphite parts used in the crystal puller hot zone. Dopant species, of course, are required by design and it turns out that some amount of interstitial oxygen is also desirable. Sufficient oxygen is desirable to provide mechanical hardening of the silicon wafer, but if too much is present it will precipitate excessively (in the form of SiO_2 inclusions) during thermal processes associated with crystal growth or semiconductor device fabrication, potentially harming the functionality of the device. This oxygen precipitation is a two-edged sword. Oxide precipitates formed in the active device region near the wafer surface can cause the device to fail but those away from the surface, in the bulk of the wafer, can provide a benefit by trapping metal impurities that may contaminate a wafer during processing. The process of trapping impurities in this way is called internal gettering. In order for gettering to take place with maximum advantage, it is necessary to ensure that oxygen precipitates form only in the wafer bulk and not near the surface. This was achieved in the 1980s by employing silicon wafers with tightly controlled oxygen levels (typically within the range ~8–15 ppma depending upon the specific application) and subjecting them to a thermal cycle at sufficiently high temperature and length of time to outdiffuse oxygen near the wafer surface such that the concentration is below the critical supersaturation level

to form precipitates. Under these conditions, during the remaining thermal processes of the device manufacturer, the oxygen near the wafer surface remains in solution while in the supersaturated wafer bulk it precipitates forming gettering centers. The near-surface region without precipitates is known as the "denuded zone" (DZ). Crystal growth processes adopted various designs, including strong magnetic fields to dampen convection within the silicon melt, to reduce and control oxygen to desired levels within 1.5 ppma. The presence of carbon and other elements was minimized, and segregation coefficients for these undesirable elements being typically of the order of 10^{-3}–10^{-7}, they preferentially segregate to the molten rather than the solid phase, ensuring that the grown crystal is even purer than the starting polysilicon.

In the 1990s, work turned to the control and engineering of agglomerated intrinsic point defects. Two types of intrinsic point defect are present in silicon, vacancies (silicon atoms missing from lattice sites) and self-interstitials in which extra silicon atoms are present at interstitial or nonlattice sites. At high temperatures, close to the melt interface, a state of dynamic equilibrium exists in which interstitials and vacancies (a Frenkel pair) are continually being created and destroyed. As the crystal cools, the transport of these defects through highly temperature-dependent diffusion and recombination mechanisms results in one species of point defect or the other predominating. If the predominant species becomes sufficiently supersaturated, the point defects can agglomerate into defect clusters. Early CZ silicon exhibited such defect clusters called A-swirl and B-swirl defects due to the swirl pattern they exhibited on wafers, and which were found to be deleterious to device fabrication.

Understanding and controlling these agglomerated defects became a major challenge and the semiconductor industry started employing high-resolution analytical techniques such as transmission electron microscopy (TEM). First detailed characterization of swirl defects were made by researchers at Philips Research Labs and Bell Telephone Labs in the early 1970s [14]–[16], who found them to be self-interstitials that had agglomerated into clusters and dislocation loops. As further improvements in CZ growth allowed for faster pull rates, a curious thing happened. The A- and B-swirl defects disappeared and were replaced by a new type of defect, called a D-defect, or later, a crystal-originated particle or pit (COP), found to be a vacancy cluster, i.e., a small void. At first, these D-defects appeared rather benign, but as device scaling drove to thinner gate oxides, they were found to cause degraded gate oxide integrity at oxide thicknesses less than ~100 nm. A breakthrough in the understanding of point defect behavior of Si was made in 1982 by Voronkov [17], who proposed a model explaining how changing silicon crystal growth conditions could change the type and concentration of predominant point defect in the crystal, a behavior unique to silicon. He recognized that the transition between interstitial-rich and vacancy-rich silicon depended on the ratio of the growth rate to the axial thermal gradient at the melt interface (V/G). For values of V/G less than a critical value, the predominant point defects would be interstitials, while for values of V/G greater than this critical value, they would be vacancies. The farther V/G is from this critical value, the larger the concentration of the predominant point defects. This work was further refined over the next ten years in collaboration with Falster [18], [19]. They realized that if (V/G) could be maintained very close to the critical value during crystal growth, the resulting vacancy and/or interstitial concentrations will remain below critical supersaturation levels, and agglomeration of these point defects will not occur. They developed predictive models to determine parameters to grow the entire crystal under conditions where V/G was close to the critical value in which a crystal free of agglomerated point defects could be grown [20], [21]. Subsequently, teams of engineers and scientists developed models in various degrees of detail and created hot zone designs which enabled such crystals to be manufactured [22].

Building on this work, a detailed understanding of the binding of vacancies by interstitial oxygen and nitrogen and its impact on both agglomerated point defect and oxygen precipitate formation was developed [23], [24]. This led to two additional approaches to defect engineering of silicon wafers. The first approach involves the deliberate doping of the silicon crystal with a small amount of nitrogen. In CZ crystals, this results in suppression of A- and B-defects, but results in a tenfold increase in D-defect density, but with much smaller size, and also greatly increases the oxygen precipitation. These last two effects are deleterious, but if the nitrogen doped wafers are subjected to a high temperature (1200 °C) anneal in argon or hydrogen, the D-defects and oxygen precipitates near the surface are dissolved, while the oxygen precipitates in the interior are grown [25]. The resulting nitrogen-doped, argon-annealed wafer has a high-quality, defect-free device region at the surface and active internal gettering sites in the bulk.

The second approach is based on the use of high-temperature (~1200 °C) rapid thermal annealing (RTA) of CZ wafers to control oxygen precipitation behavior. Frenkel pairs are formed during this RTA, and upon rapid cooling, the fast-diffusing self-interstitials diffuse to the surfaces and are lost, but the slower moving vacancies become quenched into the bulk of the wafer, except in the very near-surface regions where the vacancies can diffuse to the surface. When the wafer is reheated to modest temperatures (~800 °C) in device processing, this quenched-in vacancy template catalyzes the nucleation of oxygen precipitates in the wafer interior, providing internal gettering [26]. This magic denuded zone (MDZ) process can provide a robust, controllable oxygen precipitate density and denuded zone depth nearly independent of oxygen concentration or device thermal processing.

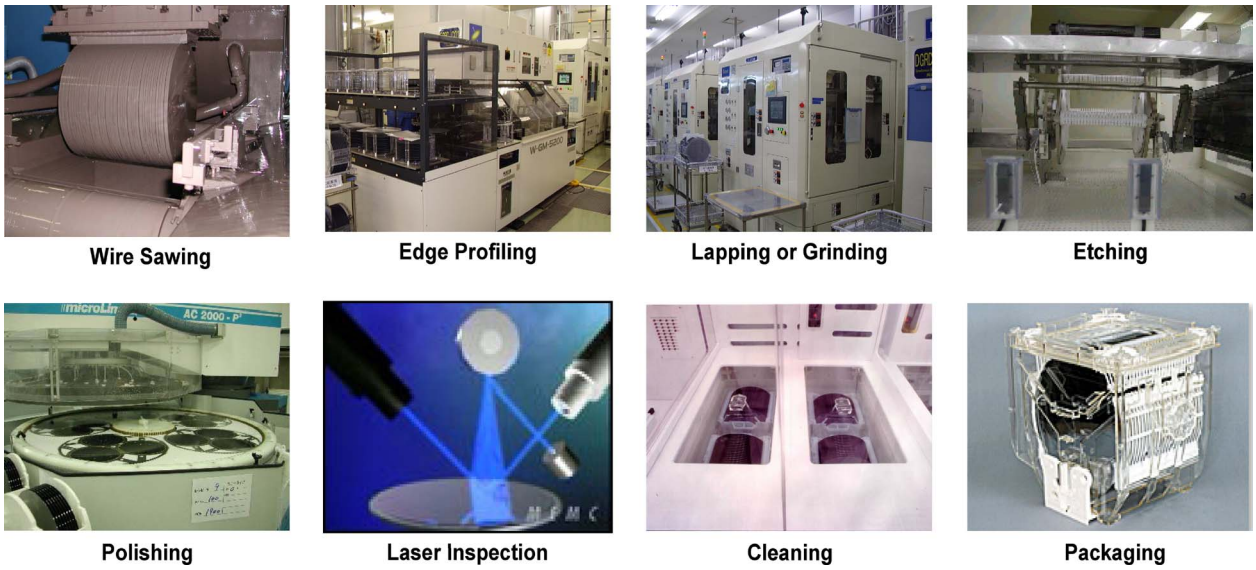


Fig. 8. *Typical processing sequence for manufacturing of semiconductor silicon wafers.*

By the end of the 1990s, the appearance of defect engineered polished substrates offered numerous advantages. Control of agglomerated point defect clusters, primarily the vacancy clusters, greatly improved gate oxide breakdown characteristics, which favored their use in many market segments, particularly for memory device manufacturers where margins are smaller and cost reduction pressures favor bulk wafer solutions over the more expensive epiwafer alternative. These products also enabled, for the first time, reliable high volume production of thin (< 100 nm) SOI wafers by layer transfer approaches such as Smartcut[1] and similar processes. When such a thin top silicon layer is transferred from a donor wafer containing D-defects, a vacancy cluster can be about the same dimension as the layer thickness, in which case, it may become a pinhole in the top silicon. Subsequent processing in a device line can lead to etching the insulating oxide through the pinhole thereby undercutting the top silicon leading to potential flaking of the layer around the defect. Commercially available defect engineered silicon wafer products such as Perfect Silicon[2] and Optia,[3] which are completely free of such defects circumvent this problem.

C. Crystal Cropping and Grinding

After the crystal has cooled, it is removed from the crystal puller for machining. In practice, diameter control tolerances of the crystal pulling stage are of the order of millimeters, which is large compared to the required diameter tolerance of finished substrates. Therefore, crystals are typically grown a few millimeters oversize on diameter and ground down to the required size prior to slicing. Initially the shoulder and tail portions are removed with a diamond blade cropping saw and recycled. The body of the crystal is then sawed into lengths that can be accommodated by the subsequent slicing operation, and prepared for grinding to the required diameter. In the days of smaller wafers a flat was ground along one side to indicate crystallographic direction as determined by X-ray diffraction but later, on larger wafers and in the interests of preserving surface area for saleable devices, the flat was replaced by a notch.

D. Slicing

The wafer production process (Fig. 8) starts with slicing of the crystal ingot. Two types of slicing methods have been used in the silicon wafer industry: the internal diameter (ID) saw and the wire saw. The ID saw uses a thin annular blade with a diamond bonded region on the inside edge of the annulus. ID saws cut only one wafer at a time, taking a few minutes to slice each wafer from the crystal. Blade flexure during slicing led to warp and bow in the resulting wafers and blade wear or poor blade dressing resulted in higher total thickness variation (TTV) from the saw. High TTV from the saw has to be corrected by the downstream processes. Saw manufacturers worked on the problem of developing tensioning systems to control flexing of the ever thinner blades required to reduce kerf losses. A wire saw on the other hand takes several hours to cut through a crystal ingot, but makes several hundred parallel saw cuts simultaneously, wafering the entire ingot in one operation (see Fig. 9). At crystal diameters larger

[1]Smartcut is a registered trademark of Soitec, France.
[2]Perfect Silicon is a registered trademark of MEMC Electronic Materials, Inc., St. Peters, MO.
[3]Optia is a registered trademark of MEMC Electronic Materials, Inc., St. Peters, MO.

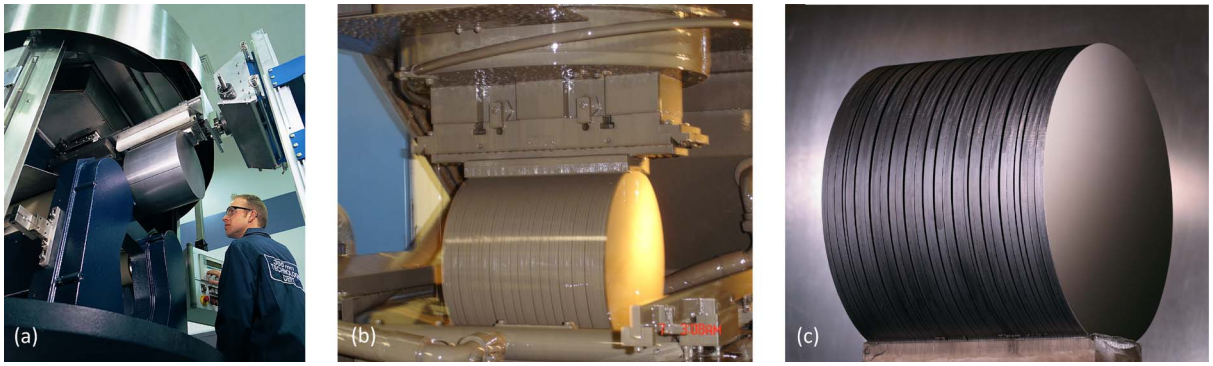


Fig. 9. *Ingots are mounted on a ceramic beam in preparation for slicing on a wire saw. (a) Uncut ingot being loaded into the saw. (b) Ingot being raised after passing through the wire slicing web. (c) The finished sliced ingot still mounted. Wafers are subsequently removed from the beam for further processing.*

than 150 mm, wire saws have proven to be more economical than ID saws with higher throughput and the potential for lower kerf losses by using thinner wires.

Wire saw slicing of silicon is achieved predominantly by free abrasive machining (FAM) using a slurry comprising silicon carbide (SiC) grit suspended in either oil or ethylene glycol. The wire acts to transport slurry to the silicon ingot where the grit becomes trapped between the tensioned wire and the ingot creating what is known as a rolling and indenting cutting mechanism [27]–[29]. Cutting speed depends on a number of factors, in particular the size and hardness of the grit and the speed of the wire which controls the rate at which grit is delivered to the cutting surface. If too much pressure is applied, the wire may distort, leading to higher TTV or warp or it may even break. In the case of silicon ingots and SiC grit, cutting speeds are typically in the region of 0.25–0.5 mm/min. Ultimately fixed abrasive cutting with diamond impregnated wire may be preferred because the induced damage is shallower, and with diamond, the cutting speed is potentially faster. The wafer industry, especially the solar wafer sector, is now adopting this technology.

Ideally, the slicing process would produce wafers with a polished surface perfectly flat and clean ready for device fabrication. In practice, as-cut wafers have significant crystallographic damage induced by the slicing process. They are typically slightly warped, of nonuniform thickness with rough, contaminated surfaces, and a square edge profile which is easily chipped. The wafering process sequence after sawing is designed to produce the ideal wafer at the lowest cost.

Machining processes that produce smooth flat polished surfaces typically have low throughputs and therefore are more expensive for a given capacity requirement because more machines are required which in turn requires more space on the factory floor, more maintenance, and potentially more operators. High throughput machines on the other hand cannot achieve the surface quality required for semiconductor wafers. As a result, a combination of machining processes is used in which the initial processes are fast, rough cuts and subsequent steps use slower cuts to remove the damage from previous steps without inducing new damage. The basic sequence of steps is shown in Fig. 1(b) starting with edge profiling, which applies a shaped grinding wheel to create a rounded wafer edge profile, which is more resistant to chipping.

E. Lapping and Etching

As-cut wafers from a saw typically have a higher TTV than that required for state-of-the-art lithographic processes used by device manufacturers. This state is corrected by subjecting the wafers to a grinding (fixed abrasive) or lapping (loose abrasive) process. The macroscopic flatness of wafers is typically determined by this lapping or grinding process. Subsequent chemical etching removes the crystallographic damage that these processes produce but care must be taken that this etching not degrade the flatness. This is achieved through choice of the etching chemistry, careful design and operation of the etching tanks, and the hydrodynamics of the etchant flow. Etchants include caustic etches such as KOH, which leave a relatively rough surface but maintain a very high degree of macroscopic flatness or acid etch, which can be optimized to produce a smoother surface but much more seriously degrades the macroscopic flatness especially near the wafer edge. The active components of acid etching are hydrofluoric and nitric acids in either acetic or phosphoric acid, which are used to tailor the viscosity. If used in the correct manner and in suitable tanks, acid etching can produce a smooth, glossy surface. A smooth backside is advantageous in that it is easier to clean, less likely to trap or generate particulates, and provides a flatter rear surface for a photolithography chuck. Consequently, acid etching is used with smaller diameter wafers (200 mm or less), which are typically only polished on the front side. The extreme demands on wafer flatness imposed by deep submicron

lithography on 300-mm wafers require a caustic etch as well as subsequent double-side polishing. The double-side polishing renders moot the issue of backside roughness created by caustic etching.

F. Polishing

With ever smaller device geometries, the wafer surface needs to be highly planar on even the smallest length scales, especially for critical photolithographic processes. The development of chemical mechanical polishing (CMP) process by Walsh in the early 1970s has been a critical enabler in manufacturing of polished wafers without microscratches or surface damage [30], [31]. CMP uses colloidal silica slurry in a basic aqueous solution to create a combination of chemical reaction and mechanical abrasion to produce a damage-free, smooth surface. Details vary but typical silicon CMP processes involve oxidation of the wafer surface by water to form silicon dioxide, abrasion of the silicon dioxide with colloidal silica, which is softer than silicon so it does not produce scratches, and etching of the exposed silicon by either potassium or sodium hydroxide.

In the traditional, single-side polishing process, wafers were mounted on a flat polishing plate with wax and the exposed surface was pressed onto a rotating polyurethane pad soaked in the silica slurry. Developments over five decades include reduction in particulate contamination, which can cause scratches, designing polishing machines with better stability, understanding and improving pad wear mechanisms and pad dressing procedures as well as optimizing pressures, temperatures, and flow rates to optimize flatness. Slurry chemistry has also been improved with various additives to increase removal rates and increase chemical purity to avoid undesirable metals such as copper.

As flatness specifications became more stringent, to accommodate the decreasing depth of field in lithography systems, the roughness of the wafer backside became a limiting factor. In the late 1990s double-side polished 200-mm wafers were introduced. Initially, these wafers were polished on the backside and then flipped over and polished on the front side in two sequential, single-side polishing steps, but very quickly simultaneous double-side polishing was introduced. Much like a lapping operation, the wafer is held in a thin carrier sandwiched between two polishing pads, and is polished on both sides simultaneously. This greatly improves the flatness and parallelism of the two polished surfaces. By the time 300-mm wafers were developed double-side polishing was the standard specification, required to meet advanced photolithography requirements.

G. Cleaning

A clean silicon surface is essential to device performance. Contaminants can cause leakage, low breakdown voltage, nonuniform oxide growth, lithography errors, and many other problems for device manufacturers. The process developed by Kern and Puotinen, which came to be called "RCA clean," in 1970 remains the basis for the processes currently used in the industry [32]. The key phases in cleaning a silicon surface are:

- removal of insoluble organic contaminants with a 5 : 1 : 1 H_2O : H_2O_2 : NH_4OH solution;
- stripping of a thin silicon dioxide layer using a diluted 50 : 1 H_2O : HF solution;
- removal of ionic and heavy metal contaminants using a solution of 6 : 1 : 1 H_2O : H_2O_2 : HCl;
- passivation of the highly reactive bare, clean, silicon surface in H_2O.

These steps are usually carried out in a high throughput automated wet bench (Fig. 10), in which a robotic carrier lifts cassettes loaded with wafers from one tank to the next. The series of tanks contain chemical solutions or deionized water (DIW). The precise details of cleaning steps used by manufacturers are usually proprietary but most are similar to the RCA clean, most developments being in the further dilution of chemicals in DIW and production of a denser cleaner native oxide during the passivation step. Clean wafers are then packed in clean shipping boxes. Packaging technology has also developed over time with improved materials and designs, which add fewer particles during shipping (Fig. 11).



Fig. 10. *A typical wet chemical bench for wafer cleaning.*

H. Epitaxy

During the first two decades of the semiconductor industry, most devices were built on polished silicon substrates, but as device densities increased and CMOS

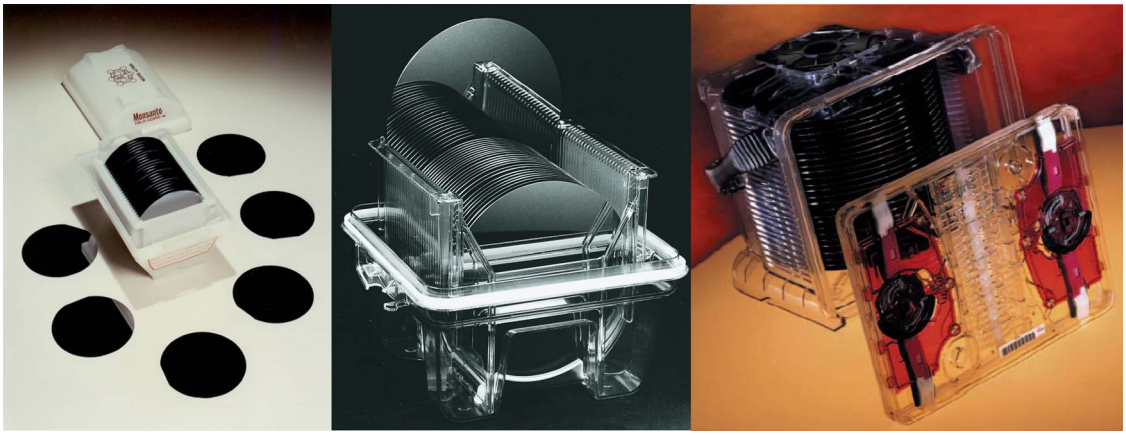


Fig. 11. *Silicon wafer shipping container circa 1970, 1990s 200-mm polycarbonate package and current generation 300-mm Front Opening Shipping Box (FOSB) package, which can be opened and closed by robotic handlers.*

architectures were adopted, epitaxial substrates became the preferred choice among advanced logic and microprocessor manufacturers. The decision on which substrate to use revolved around whether the advantages of the epitaxial wafer could justify its additional cost and, in the case of leading edge microprocessors at least, improved immunity to CMOS latch-up justified the move. Many power device designs also require silicon layer structures of differing doping densities and/or types, and once again, epitaxial structures often offer the best solution. Epitaxial wafers are also preferred for charge-coupled device (CCD) and CMOS image sensor applications.

Blanket epitaxial layer growth from chlorosilanes (usually trichlorosilane) is usually carried out at high temperatures ($>$ 1000 °C) where the deposition rate is very high (2–4 μm/min) and is controlled by the transport of gaseous phase precursors to surface. Epitaxy can be carried out at lower temperatures (as low as ~600 °C) when required, by moving from trichlorosilane to dichlorosilane to silane, but at lower temperatures, the deposition is controlled by surface reaction kinetics rather than transport phenomenon and growth rates are much slower, if polysilicon deposition is to be avoided.

III. ADVANCED SUBSTRATE TECHNOLOGIES

Today's semiconductor manufacturers are faced with a rapidly changing business environment resulting in increasing factory complexity, higher product mix operations, and intense pressure to reduce costs. Fig. 12 contrasts typical operating environments in the 1960s compared to current production. Technical challenges are many for both device and substrate suppliers, and as different solutions evolve, we see a divergence in device architectures and the substrates upon which they are built. Critical challenges are highlighted in the 2010 Technology Roadmap for Semiconductors (ITRS) (see Table 2).

A. 450-mm Substrates

Wafer diameter change requires a coordinated effort of the entire supply chain, wafer manufacturers, equipment manufacturers, and device manufacturers. While from a technical point of view there do not appear to be any fundamental barriers, engineering challenges will be significant. For the wafer suppliers, large crystal growers, crystal handling systems, thermal processing equipment (epi, RTA, furnaces), new safety considerations, wafer handling equipment, and automation systems will require a significant design effort beyond mere scaling of earlier equipment generations. Uniformity of wafer parametrics over 2$\times$ the area will present further challenges for wafer and device manufacturers and their equipment suppliers. Additionally, the introduction of 450-mm wafers will require significant effort to achieve consensus within the industry as to how to achieve economic viability of such substrates. From the device makers' standpoint, the economic presumption has traditionally been that the area of the wafer will double while the cost of the processing equipment will increase by a lesser amount (~30%) at roughly constant wafer throughput (except for photolithography, metrology, and ion implantation, which account for ever larger shares of the total process), resulting in a lower device cost on larger diameter wafers. For the wafer supplier and the equipment supplier, the scenario is much different. For the wafer supplier, it takes a much larger volume of silicon, processed at an inherently much lower throughput, to make the same surface area of silicon at larger wafer diameters than at smaller wafer diameters. Hence, the cost per unit area of larger starting wafer increases for purely physical reasons, even in the absence of enormous development and capital retooling costs that will be required. For the

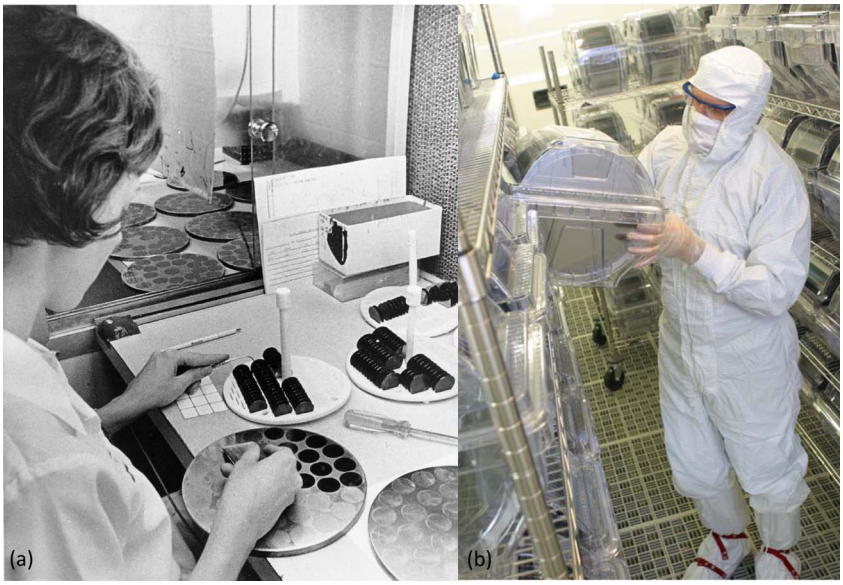


Fig. 12. ***(a) Wafers being prepared for postpolish cleaning 1960s era (vacuum tweezer handling, no gloves). (b) Wafers being prepared for processing in a later era (clean room environment).***

Table 2 International Technology Roadmap for Semiconductors (Near Term Table) 2011 Update (Copyright, ITRS, 2011, Used With Permission)

Year of Production	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*
DRAM ½ Pitch (nm) (contacted)	36	32	28	25	23	20	18
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	38	32	27	24	21	19	17
MPU Physical Gate Length (nm)	24	22	20	18	17	15	14
DRAM Total Chip Area (mm^2)	56	44	23	37	29	23	19
DRAM Active Transistor Area (mm^2)	17.8	14.1	10.4	16.4	13.0	10.4	8.2
MPU High-Performance Total Chip Area (mm^2)	260	184	260	206	164	260	206
MPU High-Performance Active Transistor Area (mm^2)	37.2	27.3	40.2	32.3	25.9	41.7	33.5
General Characteristics * (99% Chip Yield)							
Maximum Substrate Diameter (mm)—High-volume	300	300	300	450	450	450	450
Edge exclusion (mm)	2	2	2	2	2	2	2
Front surface particle size (nm), latex sphere equivalent (A)	≥45	≥45	≥32	≥32	≥32	≥22	≥22
Particles (cm^{-2}) ***	≤ 0.19	≤ 0.19	≤ 0.19	≤ 0.19	≤ 0.19	≤ 0.18	≤ 0.18
Particles (#/wf)****	≤ 134	≤ 132	≤ 131	≤ 294	≤ 291	≤ 288	≤ 285
Site flatness (nm), SFQR 26mm x 8 mm Site Size	≤36	≤32	≤28	≤25	≤23	≤20	≤18
Nanotopography, p-v, 2 mm dia. analysis area (I)	≤9	≤8	≤7	≤6	≤6	≤5	≤4
Epitaxial Wafer * (99% Chip Yield)							
Large structural epi defects (DRAM) (cm^{-2}) (B)***	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018
Large structural epi defects (MPU) (cm^{-2}) (B)***	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004
Small structural epi defects (DRAM) (cm^{-2}) (C)***	≤ 0.036	≤ 0.036	≤ 0.036	≤ 0.036	≤ 0.036	≤ 0.036	≤ 0.036
Small structural epi defects (MPU) (cm^{-2}) (C)***	≤ 0.008	≤ 0.008	≤ 0.008	≤ 0.008	≤ 0.008	≤ 0.008	≤ 0.008
Silicon-On-Insulator Wafer* (99% Chip Yield)							
Edge exclusion (mm)*****	2	2	2	2	2	2	2
Starting silicon layer thickness (Partially Depleted) (tolerance ± 5%, 3σ) (nm) (D)	46-71	43-65	40-60	38-56	35-52	33-48	31-45
Starting silicon layer thickness (Fully Depleted) (tolerance ± 5%, 3σ) (nm) (E)	17-22	17-21	16-20	15-18	14-17	14-17	14-16
Buried oxide (BOX) thickness (Fully Depleted) (tolerance ± 5%, 3σ) (nm) (F)	36-60	34-56	30-50	28-46	26-42	24-38	22-36
D_{LASOP} Large area SOI wafer defects (DRAM) (cm^{-2}) (G)***	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018
D_{LASOP} Large area SOI wafer defects (MPU) (cm^{-2}) (G)***	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004
D_{SASOP} Small area SOI wafer defects (DRAM) (cm^{-2}) (H)***	≤ 0.282	≤ 0.282	≤ 0.282	≤ 0.282	≤ 0.282	≤ 0.282	≤ 0.282
D_{SASOP} Small area SOI wafer defects (MPU) (cm^{-2}) (H)***	≤ 0.159	≤ 0.156	≤ 0.153	≤ 0.151	≤ 0.148	≤ 0.145	≤ 0.143

equipment supplier, a diameter increase incurs enormous design and development costs, which must be recouped over a smaller installed base of tools. The problem of apportionment of costs, risks, and return on investment through the supply chain in a sustainable fashion has slowed down the introduction of 450 mm, now slated for 2014. At the very least, detailed engineering cost models will need to be developed that are understood and agreed to by the entire supply chain.

Very few device manufacturers are expected to switch to the 450-mm diameter and this topic alone will present many challenges for all involved, including process and metrology tool manufacturers. While 450-mm mechanical samples are available today, there is still much to be done to reach production quality with acceptable yields, even on polished wafers. Epitaxial substrates will likely be even further behind as manufacturers tackle new layer uniformity specifications over the larger area and the new diameter will do nothing to close the cost gap between bulk and epi substrates.

B. Silicon-on-Insulator Substrates

So far SOI wafers have remained only a small fraction of the total silicon market, primarily because the cost is significantly higher than that of an epitaxial wafer. In areas such as MEMS, high voltage, optical waveguides, ultralow power, radiation hardened, and RF devices, the unique advantages of SOI justify the price differential. As capabilities improve and costs come down, we should expect the SOI wafer share to increase in other market segments.

With continued scaling beyond 22 nm, the problem of V_{th} variations due to random dopant fluctuations (RDFs) in the channel implants used to control short channel effects may become intolerable, particularly for stable static random access memory (SRAM) operation. The use of fully depleted SOI (FDSOI) transistors with undoped channels offers a potential solution. However, the threshold voltage of transistors built around FDSOI technology is a function of the top silicon layer thickness and at the 10–20-nm layer thickness required, a 1-nm thickness variation corresponds to about a 25-mV variation in V_{th}, which places tight constraints on layer thickness uniformity. Control at these levels means that the thickness uniformity requirement is approaching the scale of typical surface peak to valley roughness for layer transfer technology. FDSOI can be combined with a 10–20-nm buried oxide (BOX) layer [ultrathin body and BOX (UTB) transistors] to improve short channel effects and open up the possibility of dynamic threshold voltage control by applying back gate bias [33].

As far as silicon wafer manufacturers are concerned most of the challenges associated with the ITRS roadmap are common to both bulk and SOI solutions and, of course, qualifying SOI wafers are impossible without advanced polished wafers. Flatness specifications (including nanotopography) and particle size and number are very demanding and become more so as geometries shrink. Surface metals are also challenging, but for SOI with thin top silicon layers, surface metal specifications present additional challenges. This is because most metals landing on the top surface of thin SOI wafers get trapped in the thin silicon layer, not diffusing past the oxide. Therefore, very low surface metal concentrations can lead to high volume concentrations if diffused into a thin top layer unless surface metals are removed very effectively prior to any heating steps.

Looking at niche market sectors such as MEMS, which is inherently application specific, we will see a mix of bulk, epi, and "thick" SOI wafers. In this sector, SOI and some epitaxial wafers offer the special advantage of having a natural etch stop which cannot readily be realized in polished substrates.

C. Looking Beyond Traditional CMOS

The nonplanar transistor structures such as FinFETs (nonplanar, multigate field effect transistors where the conducting channel is a freestanding, thin silicon "fin" wrapped by a gate insulator and electrode formed on the vertical sidewalls of the fin) offer an alternative solution to the problems of RDFs and short channel effects [34], [35]. Nonplanar transistors offer several performance advantages over planar transistors, but at the cost of significant processing challenges associated with abandoning traditional planar architecture. Multigate transistors offer superior electrostatic control relative to single gate architectures. Companies are beginning to commercialize multigate transistors at the 22-nm technology node on bulk silicon wafers [36]. Their development is expected to enable extension of silicon CMOS scaling into the sub-10-nm range [37]. However, the requirements for thin silicon films and very narrow fins impose significant technical challenges to control the dimensions of the fins and control variability induced by downstream processes, both of which may cause variation in device performance that reduce the advantages gained from the FinFET. FinFETs can also be fabricated on SOI wafers, using a simpler process flow that offsets the higher cost of the SOI starting wafer.

CMOS scaling beyond FDSOI and FinFETs will likely involve the integration of higher mobility channel materials on silicon. Candidate materials include InGaAs for improving electron mobility and Ge or InSb for improving hole mobility. The comparative challenges of integrating higher mobility channel materials such as III-V or Ge in planar FDSOI structures versus in 3-D transistor structures will further complicate the choice of starting wafer. At this stage, it is impossible to predict the technical evolution and it is very likely that different device makers will adopt different solutions, and these solutions will likely require a variety of bulk and SOI substrate designs.

D. Integration With Compound Semiconductors

In many areas, silicon is likely to be the base substrate for some new materials integration. We are already seeing



Fig. 13. *This Austin Energy solar farm, built by Sun Edison, can generate up to 30 MW, enough electricity to power about 5000 homes. It is located about 20 miles east of Austin in Webberville. Its footprint covers a 380-acre site, and has 127 000 solar panels that track the sun's path. (Photos courtesy of MEMC/Sun Edison.)*

efforts to replace sapphire or silicon carbide with silicon for III-nitride materials [38]. While the barriers are formidable, due to thermal and lattice mismatches, some companies are producing GaN/Si substrates, which are initially finding use in the high-voltage power device market [39]. Further, attempts are being made to improve defect density to make them applicable for advanced devices such as high brightness light-emitting diodes (LEDs) and lasers.

In the end, each device manufacturer will find the optimum solution for its individual product mix in terms of cost and performance and it seems likely that the solutions will range across a variety of architectures and several substrates. On the other hand, it seems quite certain that silicon in one form or another will remain the semiconductor of choice for at least another decade or two with alternative materials only gaining share in niche segments of the semiconductor materials market.

IV. WAFER TECHNOLOGIES FOR PHOTOVOLTAICS

Photovoltaics (PV) constitute a large and growing market for crystalline Si (c-Si) and multicrystalline Si (mc-Si) wafers. Over the last five to six years, the role of silicon-based PV has become significantly more important for silicon wafer technology. The amount of silicon consumed in the solar industry has been rapidly growing, with PV consumption now accounting for over 80% of the worldwide production capacity of high-purity polysilicon. An example of a silicon solar power plant is shown in Fig. 13. While built on the infrastructure associated with half a century of progress in semiconductor wafer technologies, silicon PV technology is emerging as a separate R&D enterprise with its own technical and market drivers, primarily driven by the need for lower cost and high capacity.

Unlike microelectronics where the primary metric is Moore's law driven scaling and the resulting improvements in device performance, PV does not have a direct analog to device scaling. Based on the three decades of high volume PV manufacturing, the technology learning curve for Si PV (see Fig. 14) shows that the price of technology ($/Wp) has decreased by 20% for each doubling of cumulative installed capacity [40], [41]. The challenge is to sustain this rate of technology and cost improvements, and bring PV to grid parity without feed-in-tariffs and other subsidies. With limited opportunity for dramatic improvements in PV efficiency, there is an industry-wide push to reduce the active Si content of the cell in combination with improved light management.

One of the critical drivers for crystalline Si is the need to achieve grid parity and to make PV competitive with power grid retail prices. While achieving grid parity will need a regulatory framework that allows for optimal deployment of resources, reducing materials and manufacturing costs also needs to occur. With increased manufacturing volumes, there is limited scope for cost reduction through

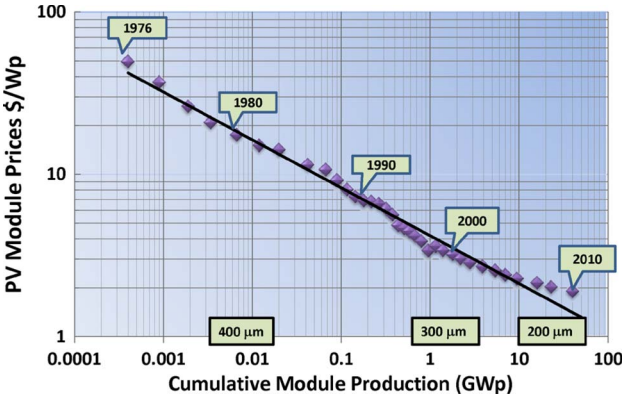


Fig. 14. *Price learning curve for crystalline Si modules as function of installed capacity. (Data sources: National Renewable Energy Laboratory, European Photovoltaic Industry Association, Navigant Consulting.)*

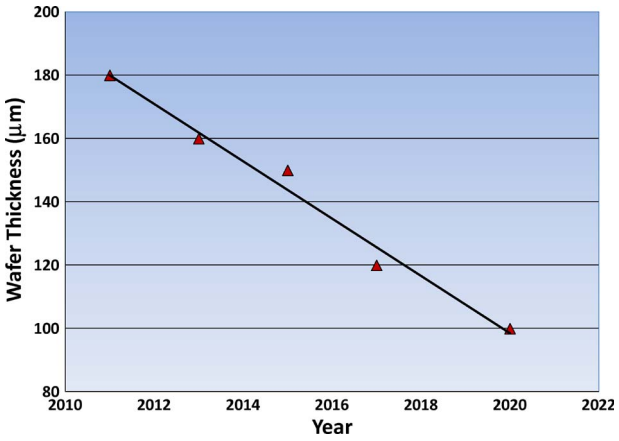


Fig. 15. *Projected trend in minimum wafer thickness processed in mass production of solar cells. (International Technology Roadmap for Photovoltaics, SEMI PVGroup/ITRPV, 2011.)*

manufacturing efficiencies alone; the input cost of module materials, especially the amount of Si used, becomes a bigger factor.

Thus, at the wafer level, reducing the consumption of silicon is one of the main drivers for solar wafers, so is the need for new and improved silicon feedstock and wafer (and wafer equivalent) manufacturing technologies.

A. Trends in Crystalline Silicon Photovoltaics

Efficiency of commercial modules with single crystal Si (sc-Si) and multicrystalline Si (mc-Si) wafers are in the 18%–24% and 14%–18% ranges, respectively. Wafer thickness has reached below 200 μm, corresponding to silicon material use of about 5 g/Wp. Since the silicon wafer is the largest cost component of finished solar cell, it is widely accepted that reducing the cost of silicon through reduced wafer thicknesses will greatly benefit lower solar energy costs. Further reduction would require improvements in wafering processes and the development of new and alternate wafering technologies. Past cost reductions in crystalline Si PV were mainly achieved by reducing the cost per area rather than by improving the power output per area. For crystalline Si, the reduction of cost per area will, in the long run, remain a key challenge due to the fundamental limitation on maximum solar cell efficiency. But, there is no clear consensus on how far current c-Si wafer technology can be driven before we hit the brick wall and the point where kerf losses, yield issues, or handling of thin wafers become real bottlenecks. Based on technology roadmaps from the International Energy Agency (IEA), and trade groups such as Semiconductor Equipment and Materials International (SEMI) and European Photovoltaic Industry Association (EPIA) (see Table 3), we can summarize the general trends [42].

Currently, commercial PV wafers produced with wire slicing range in nominal thickness from about 150 to 200 μm. However, reducing the thickness of wafers further is a manufacturing challenge, with increasing kerf loss, reduced yield due to breakage, and more stringent wafer handling requirements. For wafer thickness reduction, the two key elements are the cost of silicon and the ability to mitigate yield losses due to microcracks. Trends in wafer thickness estimates for the next ten years are shown in Fig. 15. The various industry roadmaps project wafer thickness to reach 100 μm, possibly near the limit of wire slicing technology, by the end of the decade. Further reduction will require development of wafer equivalent technologies such as layer transfer techniques or epitaxial growth of thin wafers.

B. Multicrystalline Wafer Technology

Semiconductor grade wafers are not needed for solar. Unlike CZ growth of ingots, casting offers a lower cost approach for large ingot growth. One of the most common approaches for large multicrystalline ingot casting is through directional solidification of silicon (DSS) [43], [44]. There have been significant advances in DSS technology that allows for casting larger charge size multicrystalline ingots, improved crystalline quality, and significantly reduced cost of ownership. For example, Fig. 16 highlights the exceptional progress in manufacturing, with the size of the mc-Si ingots increasing from 270 kg in 2006 to almost 2 tons in 2010. These large ingots allow for more wafers per cast, improved yields, and the potential for sizing wafers to larger dimensions (although the latter is currently not envisioned). Although there seem to be no industry-wide plans to go beyond 156-mm wafers, larger ingots do offer significant manufacturing improvements through increased wafer output per cast ingot.

Within the last two years, mc-Si solar cell volume has expanded significantly and now has a larger market share than c-Si cells. The efficiency gap between c-Si and mc-Si cells has decreased considerably [45]. There is

Table 3 Crystalline Silicon Substrate Technology Roadmap for Photovoltaics. (Summary From IEA/SEMI/EPIA, 2011)

Crystalline Silicon Technology	2010 - 2015	2015 - 2020	2020 – 2030/50
Efficiency Targets for commercial modules(%)	♦ Single crystal 21% ♦ Multi crystal: 17%	♦ Single crystal 23% ♦ Multi crystal: 19%	♦ Single crystal 25% ♦ Multi crystal: 21%
Industry Manufacturing Aspects	♦ Silicon consumption <5gm/W	♦ Silicon consumption <3gm/W	♦ Silicon consumption <2gm/W
Selected R&D Areas	♦ New silicon materials and processing ♦ Cell contacts, emitters and passivation	♦ Improved device structures ♦ Productivity and cost optimization in production	♦ Wafer equivalent technologies ♦ New device structures with novel concepts

considerable opportunity for DSS technology to improve wafer quality by reducing dislocation density, increasing grain size, and reducing the carbon concentration below saturation level [46]. Multi- and monocrystalline wafers and cells are shown in Fig. 17.

C. Continuous Czochralski Crystal Growth (CCZ)

One of the main challenges with traditional CZ is the low throughput of this inherently batch process. In CCZ, continuous resupply of fresh polysilicon maintains constant melt height in the crucible, and high-purity resupply dilutes impurity buildup due to segregation phenomena. Continuous production ensures far better utilization of raw silicon feedstock, a tighter control of dopant concentration, and competitive costs. As the wafer quality is similar to semiconductor grade wafers, enhanced electrical performance of each premium wafer allows solar cell manufacturers to create higher efficiency cells with competitive wafer costs.

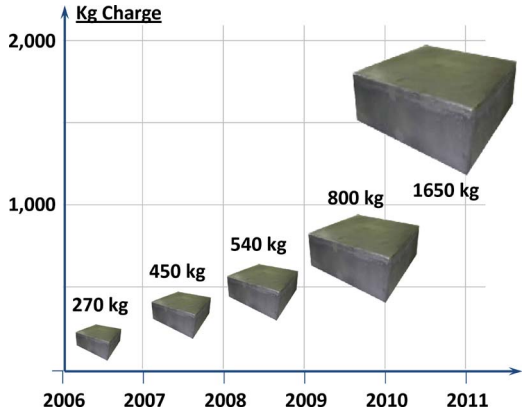


Fig. 16. *Growth over the last five years in the size of ingots cast using DSS. (Courtesy of MEMC.)*

D. Silicon Ribbons

Drawing ribbon directly from silicon melt has been used to grow large strings of thin Si [47]. This process allows for faster growth, with the ability to grow long ribbons reaching into 100-m range. But the technique does not lead to high-quality crystals; the polycrystalline ribbons tend to have high-defect densities leading to reduced efficiencies, and the unique wafers produced by this method generally require a specialized solar cell manufacturing process. String ribbon will remain a niche as the technology requires different manufacturing processes than the existing silicon-wafer-based manufacturing infrastructure.

E. Wafer-Like Technologies

Reducing the solar cell thickness improves the diffusion-length-to-cell-thickness ratio, thus improving the overall cell efficiency potential. With adequate light trapping and very good surface passivation, cell efficiency peaks in the 20–50-μm thickness range [48], [49]. Fig. 18 gives cell efficiency as a function of cell thickness, which shows efficiency peaking around 40-μm silicon thickness.

To reduce material use, there continues to be activity in developing methods to obtain high-quality thin c-Si wafers [50]–[52]. Development of thin crystalline silicon wafers promises to offer substantial reduction of Si material consumption in solar cells, while maintaining efficiencies comparable to thicker c-Si solar cells. A number of techniques are being explored to produce thin crystalline

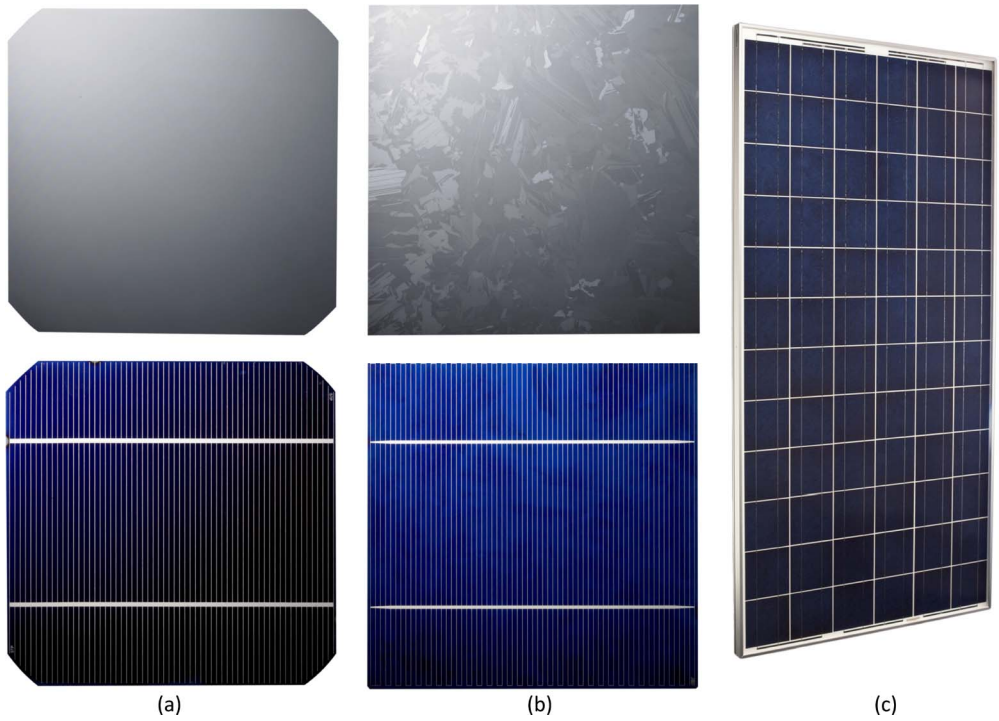


Fig. 17. *Two types of silicon wafers for solar cells: (a) 156-mm monocrystalline solar wafer and cell; (b) 156-mm multicrystalline solar wafer and cell; and (c) 280-W solar cell module (from multicrystalline wafers).*

silicon wafers. These include epitaxial growth and various exfoliation techniques that use ion implant, stress engineering, or electrochemical means to separate a thin crystalline layer from the parent substrate. While there has been significant progress in demonstrating thin c-Si cells using these techniques, further improvements are needed for commercialization.

Epitaxial growth is capable of producing high-quality c-Si layers on large areas using high growth rate CVD deposition techniques. Liftoff or layer transfer technologies allows the epitaxial layer to be detached from a reusable monosilicon substrate, while still maintaining the high quality of the film. One such approach is epitaxial silicon growth on a porous-Si substrate followed by separation along the epi/porous-Si interface, attachment of the epitaxial foil to a support substrate for cell processing, and reuse of the original silicon substrate. Challenges to this approach include handling of the fragile thin crystalline wafers, and meeting the yield, cost, and throughput requirements for the epitaxial growth and separation processes.

The ion implant assisted exfoliation process applied to silicon blocks involves the use of high-energy proton ion implantation to create a weakened region in the silicon bulk at a depth determined by the ion implant energy. Wafers are then separated from the silicon block by cleavage along the weakened ion implant plane. The process proceeds with sequential implants and separations until the silicon block is consumed [53]. Challenges include handling the thin silicon foils, making them into high efficiency cells, thermal annealing to recover the degradation of carrier lifetime due to implant damage, and the cost and throughput challenges associated with sequential high-energy implantation and wafer separation.

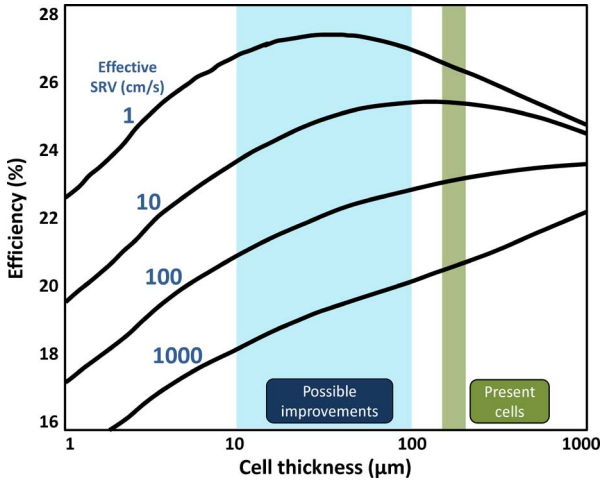


Fig. 18. *With sufficient passivation to reduce surface recombination velocity, cell efficiency may be optimized with cell thickness of around 20–60 μm [48], [49]. (Courtesy of Jerry Fossum, University of Florida and Stuart Bowden, Arizona State University.)*

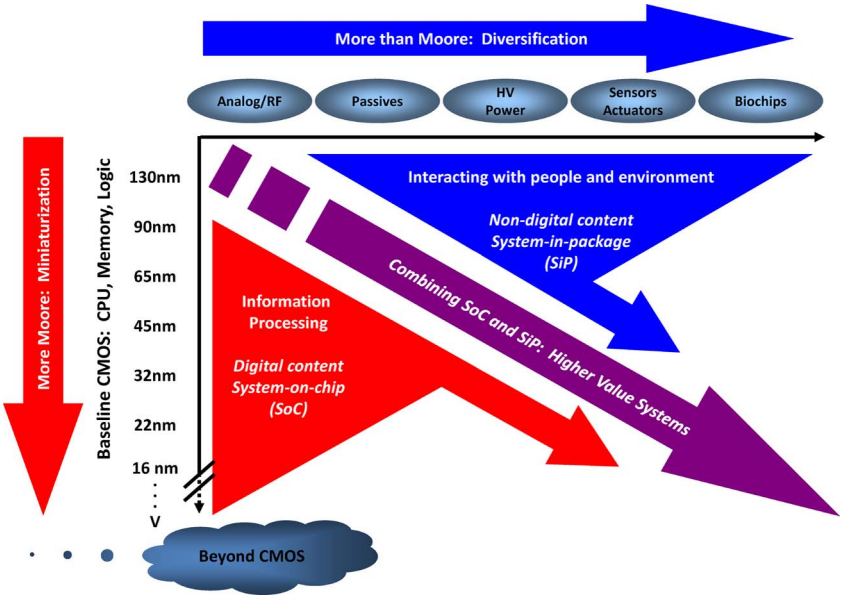


Fig. 19. ***Diverging trend lines in International Technology Roadmap for Semiconductors: miniaturization of the digital functions ("More Moore") and functional diversification ("More-than-Moore"). (Copyright ITRS, 2010, used with permission.)***

V. FUTURE TRENDS

The driving force for the microelectronics industry over the last 40 years has been the relentless increase in integration density enabled by dimensional scaling and coupled with the transistor performance benefits associated with reducing metal–oxide–semiconductor field-effect transistor (MOSFET) critical dimensions [54]–[56]. The entire industry supply chain from raw material suppliers to equipment manufacturers to device makers have shared a common industry roadmap that has charted the course for continued miniaturization and increased transistor performance and chip functionality. In recent years when traditional transistor dimensional scaling was no longer sufficient to maintain this progress, new materials and device structures were integrated into the silicon-based device platform to sustain performance scaling [57]. It is expected the trends of miniaturization and increasing performance will continue within the constraints of performance versus power tradeoffs (see Fig. 19). This trend for continued progress in digital content scaling has been described as "More Moore" [58]. For the silicon wafer supplier, "More Moore" continues the roadmap for flatter, cleaner, lower defect density wafers that enable smaller feature sizes and pitches at high manufacturing yields. It will eventually drive toward the larger diameter 450-mm wafer size for a select few device makers. The trend toward new device architectures for performance scaling, such as FDSOI and FinFETs, will result in continued diversification of wafer platforms between bulk silicon, epitaxy, and SOI. FDSOI-type wafers impose challenges on the manufacturing of ultrathin SOI layers (ca. < 20 nm), likely on thin BOX layers (ca. < 50 nm). Beyond the 10-nm node, researchers are working toward high mobility nonsilicon channel material integration on silicon for continued performance scaling.

A more recent important trend in semiconductor devices is the increased level of heterogeneous integration of diverse device types that add system functionality. Examples are the combinations of traditional digital functions such as central processing unit (CPU) with nondigital functions such as analog/mixed signal/RF, high voltage, passives, and sensors. The combination of these functions has typically been realized at the package level, but multiple functions are increasingly combined in "system-on-chip" approaches on single die. The trend for increasing integration of diverse device types to increase functionality has been described as "More than Moore." Silicon wafer designs will naturally vary for such a diverse set of device types. Wafer requirements will be dictated much more by the device function than by dimensional scaling.

As silicon-based power devices approach their fundamental performance limits in the next few years it is possible that GaN, a wide bandgap, high mobility semiconductor, grown on silicon may achieve increased penetration into the traditional silicon high-voltage power device market. Early commercial devices have been introduced into the market. GaN on silicon power devices achieve much lower on-resistance for a given breakdown voltage and are capable of higher frequency, high-efficiency power switching. Large diameter GaN epi growth on silicon is challenging due to the thermal and lattice mismatches that exist between the two materials. However, progress in

reducing dislocation density and controlling wafer warp could lead to GaN grown on large diameter silicon as alternative to GaN on sapphire in the growing LED device market.

III-nitrides crystallized in the wurtzite structure have dangling bonds available for interaction with various base ligands depending upon the precise surface chemistry. GaN has already been used for chemical field-effect transistors (CHEMFETs), in which the proximity of Lewis bases causes band bending which impacts the current flowing through the device [59], [60]. Other new devices like biosensors and direct biochemical analysis will likely be developed around nanotechnology involving quantum dots, nanoporous materials, and materials involving nanorods and nanocolumns. New materials like organic materials or molecular electronics have been researched for some time and are still some years away from commercialization. In the case of molecular electronics, for example, we still need to know much more about self-assembly, transport properties, and how to make suitable contacts, and fundamental issues like temperature dependences and the impact of electron transport on the chemical properties of the molecules. Over the next decade or so infrastructures around some of these new materials will be developed just as they were around silicon. As we learn how to manipulate these materials to take full advantage of their properties, new devices and their commercialization will follow.

For MOSFET transistors with channel lengths smaller than 10 nm it is anticipated that nonsilicon channel materials will be required to maintain performance scaling. As discussed previously, this may represent the point for introduction of high carrier mobility compound semiconductor channel materials such as InGaAs, InSb, or Ge [61], [62]. Current integration schemes are mostly focused on selective epitaxial growth of complex layer stacks during device fabrication, which are engineered to mitigate lattice mismatch issues with the silicon substrate. Transistor performance scaling may ultimately lead to carbon nanotube transistors (CNTs) on silicon. Researchers have demonstrated wafer scale, oriented CNT growth on quartz substrates followed by a transfer process to a silicon substrate, and subsequently the fabrication of sub-10-nm CNTs with promising transistor scaling behavior [63]–[66]. Another carbon-based material of intense research interest is graphene. It exhibits a remarkable combination of electronic, mechanical, thermal, and optical properties. Although the absence of a native bandgap may limit its suitability for digital transistor scaling, graphene's extremely high mobility makes it an attractive candidate for eventually scaling RF transistor operating frequency to the terahertz range [67], [68]. Much work remains to develop manufacturable methods for growing large area graphene and then integrating it on silicon [69], [70].

Should carbon nanotubes, graphene, molecular semiconductors, or some other exotic material become the material of choice for the active devices of the sub-10-nm era, it is still likely that the substrate to support these materials will be silicon. The large wafer diameters, crystalline perfection, ultrahigh purity, mechanical and chemical robustness, extreme flatness and cleanliness and high-quality oxide insulator afforded by semiconductor silicon, combined with a rich infrastructure of deposition, etching and patterning processes and tools, guarantees silicon a central role in semiconductor device technology far into the future. ■

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